Best Available Copy

Commonwealth of Australia

Letters patent

Patents Act 1990

No. 775072

STANDARD PATENT

I, Fatima Beattie, Commissioner of Patents, grant a Standard Patent with the following particulars:

Name and Address of Patentee:
Leviton Manufacturing Co., Inc., 59-25 Little Neck Parkway Little Neck NY 11362 United States Of America

Names of Actual Inventors: Nicholas L. Disalvo; William R. Ziegler; Frantz Germain; David Herzfeld; Stephen Stewart and Roger M. Bradley

Title of Invention: Circuit breaker with independent trip and reset lockout

Application Number: 67945/00

Term of Letters Patent: Twenty years from 18 August 2000

Priority Details:

Number	*Date*	*Filed with*
09/379140	20 August 1999	UNITED STATES OF AMERICA

Dated this 28 day of October 2004

F. BEATTIE
COMMISSIONER OF PATENTS

(12) **PATENT**
(19) **AUSTRALIAN PATENT OFFICE**

(11) Application No. **AU 200067945 B2**
(10) Patent No. **775072**

(54) Title
Circuit breaker with independent trip and reset lockout

(51)[7] International Patent Classification(s)

H01H 009/02	H01H 081/00
H01H 009/08	H01H 083/00
H01H 013/04	H01H 083/06
H01H 073/00	H01H 085/00
H01H 073/02	H02H 003/00
H01H 073/12	H02H 003/16
H01H 073/48	H02H 003/26
H01H 075/00	H02H 003/32
H01H 077/00	H02H 009/08

(21) Application No: **200067945**

(22) Application Date: **2000.08.18**

(87) WIPO No: **WO01/15183**

(30) Priority Data

(31) Number	(32) Date	(33) Country
09/379140	1999.08.20	US

(43) Publication Date : **2001.03.19**
(43) Publication Journal Date : **2001.05.24**
(44) Accepted Journal Date : **2004.07.15**

(71) Applicant(s)
Leviton Manufacturing Co., Inc.

(72) Inventor(s)
Nicholas L. Disalvo; William R. Ziegler; Frantz Germain; David Herzfeld; Stephen Stewart; Roger M. Bradley

(74) Agent/Attorney
Davies Collison Cave,GPO Box 3876,SYDNEY NSW 2001

(56) Related Art
US 5655648
GB 2290181
US 4851951

AU 200067945

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 March 2001 (01.03.2001)

PCT

(10) International Publication Number
WO 01/15183 A3

(51) International Patent Classification[7]: H01H 9/02, 9/08, 13/04, 73/00, 73/02, 73/12, 73/48, 75/00, 77/00, 81/00, 83/00, 83/06, 85/00, H02H 3/00, 3/16, 3/26, 3/32, 9/08

(21) International Application Number: PCT/US00/22955

(22) International Filing Date: 18 August 2000 (18.08.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/379,140 20 August 1999 (20.08.1999) US

(71) Applicant: LEVITON MANUFACTURING CO., INC. [US/US]; 59-25 Little Neck Parkway, Little Neck, NY 11362 (US).

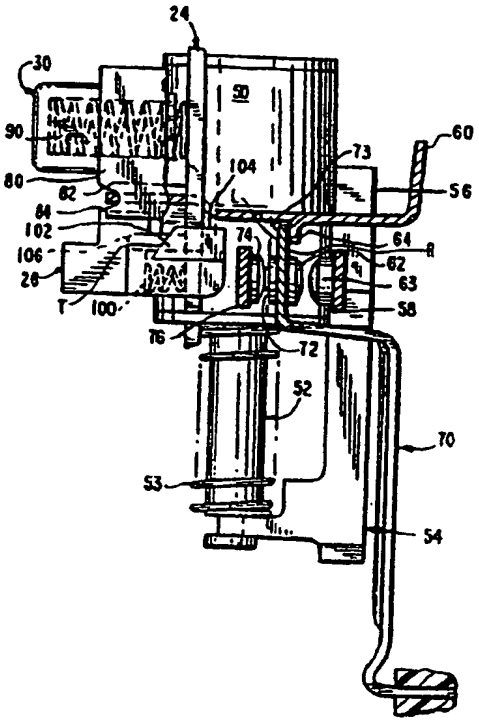
(72) Inventors: DISALVO, Nicholas, L.; 61 Primrose Lane, Levittown, NY 11756 (US). ZIEGLER, William, R.; 6 Clarisse Lane, East Northport, NY 11731 (US). GERMAIN, Frantz; 142-10 243rd Street, Rosedale, NY 11422 (US). HERZFELD, David; 8 Woodhollow Lane, Huntington, NY 11743 (US). STEWART, Stephen; 721 Colonial Street, Uniondale, NY 11533 (US). BRADLEY, Roger, M.; 2071 Decatur Avenue, North Bellmore, NY 11710 (US).

(74) Agents: SUTTON, Paul, J. et al.; Greenberg Traurig, LLP, 885 Third Avenue, New York, NY 10022 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ,

[Continued on next page]

(54) Title: CIRCUIT BREAKER WITH INDEPENDENT TRIP AND RESET LOCKOUT



(57) Abstract: Resettable circuit breakers (10) having an independent trip mechanism (26) and a reset lockout (60) are provided. The trip mechanism operates (26) independently of the fault protection operations, and the reset lockout (60) prevents the resetting of the circuit breaker if the fault protection is non-operational or if an open neutral exists.

WO 01/15183 A3

NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*

(88) **Date of publication of the international search report:**
20 September 2001

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US00/22955

A. CLASSIFICATION OF SUBJECT MATTER
IPC(7) : H01H 9/02, 9/08, 13/04, 73/00, 73/02, 73/12, 73/48, 75/00, 77/00, 81/00, 83/00, 83/06, 85/00; H02H 3/00, 3/16, 3/26, 3/32, 9/08
US CL : 361/42, 43, 44, 45, 46, 47, 48, 49, 50; 335/18, 21, 24, 25, 26, 202

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 361/42, 43, 44, 45, 46, 47, 48, 49, 50; 335/18, 21, 24, 25, 26, 202

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4,595,894 A (Doyle et al.) 17 June 1986 (17.06.1986), See Figures 1, 6, 7 and 8.	1-23, 33-42, 46-57, 62-75
Y	US 4,851,951 A (Foster, Jr.) 25 July 1989 (25.07.1989), see Column 3, lines 47-63.	1-23, 33-42, 46-57, 62-75
Y	US 5,600,524 A (Neiger et al.) 04 February 1997 (04.02.1997), see Column 3, lines 6-59, Column 4, lines 19-33 and Column 6, line 60 through Column 7, line 40.	4, 14, 35, 40, 52, 64
A		24-32,43-45,58-61

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
22 September 2000 (22.09.2000)	06 DEC 2000
Name and mailing address of the ISA/US Commissioner of Patents and Trademarks Box PCT Washington, D.C. 20231 Facsimile No. (703)305-3230	Authorized officer Ronald W. Haga Telephone No. (703)308-3408

Form PCT/ISA/210 (second sheet) (July 1998)

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
1 March 2001 (01.03.2001)

PCT

(10) International Publication Number
WO 01/15183 A2

(51) International Patent Classification[7]: H01H

(21) International Application Number: PCT/US00/22955

(22) International Filing Date: 18 August 2000 (18.08.2000)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
09/379,140 20 August 1999 (20.08.1999) US

(71) Applicant: LEVITON MANUFACTURING CO., INC. [US/US]; 59-25 Little Neck Parkway, Little Neck, NY 11362 (US).

(72) Inventors: DISALVO, Nicholas, L.; 61 Primrose Lane, Levittown, NY 11756 (US). ZIEGLER, William; R.; 6 Clarissa Lane, East Northport, NY 11731 (US). GERMAIN, Frantz; 142-10 243rd Street, Rosedale, NY 11422 (US). HERZFELD, David; 8 Woodhollow Lane, Huntington, NY 11743 (US). STEWART, Stephen; 721 Colonial Street, Uniondale, NY 11533 (US). BRADLEY, Roger, M.; 2071 Decatur Avenue, North Bellmore, NY 11710 (US).

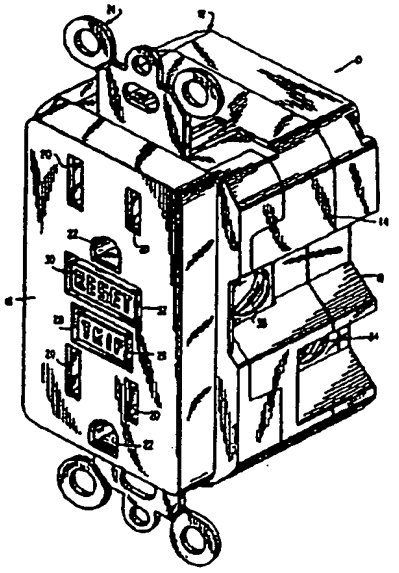
(74) Agents: SUTTON, Paul, J. et al.; Greenberg Traurig, LLP, 885 Third Avenue, New York, NY 10022 (US).

(81) Designated States *(national)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CR, CU, CZ, DE, DK, DM, DZ, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA, ZW.

(84) Designated States *(regional)*: ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

[Continued on next page]

(54) Title: CIRCUIT BREAKER WITH INDEPENDENT TRIP AND RESET LOCKOUT



(57) Abstract: Resettable circuit breakers having an independent trip mechanism and a reset lockout are provided. The trip mechanism operates independently of the fault protection operations, and the reset lockout prevents the resetting of the circuit breaker if the fault protection is non-operational or if an open neutral condition exists.

WO 01/15183 A2

Published:
— *Without international search report and to be republished upon receipt of that report.*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

CIRCUIT BREAKER WITH INDEPENDENT TRIP AND RESET LOCKOUT

BACKGROUND

1. Field

The present application relates to a family of resettable circuit breakers that include a reset lockout operation and optionally an independent trip operation, and to power distribution systems in which such circuit breakers are utilized. More particularly, the present application is directed to circuit breakers that include a reset lock out capable of preventing the circuit breaker from resetting if a circuit interrupting portion used for fault protection is not functioning properly and/or if an open neutral condition exists. In addition, a trip portion may be added to the circuit breaker to permit the breaker to be tripped independent of the operation of the circuit interrupting portion.

2. Description of the Related Art

The electrical wiring device industry has witnessed an increasing call for circuit interrupting devices or systems which are designed to interrupt power to various loads, such as household appliances, consumer electrical products and branch circuits. In particular, electrical codes require electrical circuits in home bathrooms and kitchens to be equipped with ground fault circuit protection. Presently available GFCI devices, such as the GFCI receptacle described in commonly owned U.S. Patent 4,595,894, use an electrically activated trip mechanism to mechanically break an electrical connection between one or more input and output conductors. Such devices are resettable after they are tripped by, for example, the detection of a ground fault. In the device discussed in the '894 patent, the trip mechanism used to cause the mechanical breaking of the circuit (i.e., the connection between input and output conductors) includes a solenoid (or trip coil). A test button is used to test the trip mechanism and circuitry used to sense faults, and a reset button is used to reset the electrical connection between input and output conductors.

However, instances may arise where an abnormal condition, caused by for example a lightning strike, occurs which may result not only in a surge of electricity at the device and a tripping of the device but also a disabling of the trip mechanism used to cause the breaking of the circuit. This may occur without the knowledge of the user. Under such circumstances, an unknowing user faced with a GFCI which has tripped may press the reset button which, in turn, will cause the device with an inoperative trip mechanism to reset without the ground fault protection available.

Further, an open neutral condition, which is defined in Underwriters Laboratories (UL) Standard PAG 943A, may exist with the electrical wires supplying electrical power to such GFCI devices. If an open neutral condition exists with the neutral wire on the line (versus load) side of the GFCI device, an instance may arise where a current path is created from the phase (or hot) wire supplying power to the GFCI device through the load side of the device and a person to ground. In the event that an open neutral condition exists, current GFCI devices which have tripped, may be reset even though the open neutral condition may remain.

Commonly owned Patent No. 6,040,967, issued March 21, 2000, which is incorporated herein in its entirety by reference, describes a family of resettable circuit interrupting devices capable of locking out the reset portion of the device if the circuit interrupting portion is non-operational or if an open neutral condition exists. Commonly owned application Serial No. 09/175,228, filed October 20, 1998, which is incorporated herein in its entirety by reference, describes a family of resettable circuit interrupting devices capable of locking out the reset portion of the device if the circuit interrupting portion is non-operational or if an open neutral condition exists and capable of breaking electrical conductive paths independent of the operation of the circuit interrupting portion.

Current resettable circuit breakers with fault protection capabilities, such as the HOM-GFI series of GFCI circuit breakers manufactured by Square-D Company, Palatine, Illinois, have line and load power and neutral connections and a switch for controlling power distribution to a load. To provide fault protection, such circuit breakers have sense circuitry and linkage to the switch, which are capable of sensing faults (e.g., ground faults) between the load power and the line neutral conductors and opening the switch. A test

button accessible from an exterior of the breaker is used to test the operation of the fault protection portion of the breaker when depressed. However, like conventional resettable receptacles, conventional resettable circuit breakers do not include either a reset lockout or an independent trip portion.

5

SUMMARY

The present application relates to a family of resettable circuit breakers having fault protection capabilities. The circuit breakers according to the present application include a circuit interrupting portion, a reset portion and a reset lockout portion. The circuit breakers may also include an independent trip portion. The reset lockout portion inhibits the resetting of the circuit breaker if the circuit interrupting portion is non-operational or if an open neutral condition exists. The trip portion operates independently of the circuit interrupting portion and facilitates tripping of the circuit breaker whether or not the circuit interrupting portion is operating properly.

In one embodiment, a GFCI circuit breaker having a housing, a circuit interrupting portion, a reset portion and a reset lockout portion is provided. Preferably, the housing has line phase and load phase connections that are accessible from an exterior of the housing and a conductive path within the housing between the line and load phase connections. The circuit interrupting portion is disposed within the housing and is configured to open the conductive path upon the occurrence of a ground fault. Examples of faults contemplated include ground faults, arc faults, immersion detection faults, appliance leakage faults and equipment leakage faults. The reset portion includes an actuator that is also accessible from the exterior of the housing, and is configured to close the conductive path upon actuation. Preferably, the reset lockout portion inhibits the closing of the conductive path if the circuit interrupting portion is non-operational or if an open neutral condition exists. The reset lockout portion may be an active type lockout that prevents the resetting of the conductive path, or a passive type lockout whose characteristics inherently inhibit the resetting of the conductive path.

The circuit breaker may optionally include a trip portion disposed at least partially within the housing. The trip portion is configured to open the conductive path independently of the operation of the circuit interrupting portion. Thus, in this configuration, if the circuit interrupting portion is not operating properly, the circuit breaker can still be tripped but it cannot be reset, since the reset operation utilizes the circuit interrupting portion when resetting the breaker.

The present application also provides a method for testing the operation of a circuit breaker having a housing with line and load phase connections accessible from an exterior surface of the housing, and a conductive path between the line and load phase connections. The method includes the steps of: 1) manually activating a trip portion of the circuit breaker to open the conductive path and to enable a reset lockout portion that inhibits closing the conductive path; and 2) activating a reset portion to perform a reset operation. During the reset operation a circuit interrupting portion is activated, and if the circuit interrupting portion is operational the circuit interrupting portion disables the reset lockout portion and facilitates closing of the conductive path. If, however, the circuit interrupting portion is not operating properly, the reset lockout portion remains enabled so that closing the conductive path is inhibited.

The present application also provides a circuit interrupting system that includes a source of power, a circuit breaker, having for example the above described independent trip and reset lockout portions, connected to the source of power, and at least one load connected to the circuit breaker.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the present application are described herein with reference to the drawings in which similar elements are given similar reference characters, wherein:

Fig. 1 is a perspective view of an exemplary ground fault circuit interrupting device according to the present application;

Fig. 2 is side elevational view, partly in section, of components of an independent trip mechanism and a reset mechanism for the GFCI device shown in Fig. 1, illustrating the components when the circuit interrupting device is in a set or circuit making position;

Fig. 3 is a side elevational view similar to Fig. 2, illustrating components of the independent trip mechanism when the circuit interrupting device is in a circuit breaking position;

Fig. 4 is a side elevational view similar to Fig. 2, illustrating the components of the reset mechanism during reset operation of the circuit interrupting device;

Figs. 5-7 are schematic representations of one embodiment of the reset mechanism of the present application, illustrating a latching member used to make an electrical connection between input and output conductors and to relate the reset mechanism with the operation of the circuit interrupter;

Fig. 8 is a schematic diagram of a circuit for detecting ground faults and resetting the circuit interrupting device of Fig. 1;

Fig. 9 is side elevational view, partly in section, of components of an alternative embodiment of the independent trip mechanism, illustrating the components when the circuit interrupting device is in a set or circuit making position;

Fig. 10 is a side elevational view similar to Fig. 9, illustrating components of the alternative independent trip mechanism when the circuit interrupting device is in a circuit breaking position; and

Fig. 11 is a block diagram of a circuit interrupting system according to the present application that incorporates a ground fault circuit interrupter receptacle;

Fig. 12 is a perspective view of an exemplary ground fault circuit interrupting circuit breaker according to the present application;

Fig. 13 is a cross sectional view of the GFCI circuit breaker of Fig. 12, taken along line A-A, illustrating the breaker in an 'on' state;

Fig. 14 is a cross sectional view of the GFCI circuit breaker of Fig. 12 similar to Fig. 13 and illustrating the breaker in a 'tripped' state;

Fig. 15 is a cross sectional view of the GFCI circuit breaker of Fig. 12 similar to Fig 13 and illustrating the breaker with the reset lockout in a lockout position;

Fig. 16 is a cross sectional view of the GFCI circuit breaker of Fig. 12 similar to Fig. 15 and illustrating the reset lockout removed from the lockout position;

Fig. 17 is a cross sectional view of the GFCI circuit breaker of Fig. 12 similar to Fig. 13 and illustrating the breaker in an 'off' state;

Fig. 18 is a cross sectional view of the GFCI circuit breaker of Fig. 12 similar to Fig. 13 and illustrating partial activation of the independent trip portion of the breaker;

Figs. 19 and 20 are circuit diagrams for various embodiments of the sensing circuitry used to sense ground faults and switching configurations for a reset enable switch assembly used when resetting the circuit breaker;

Fig. 21 is another alternative switching configuration for the reset enable switch assembly used when resetting the circuit breaker;

Fig. 22 is a block diagram for the fault sensing circuitry for detecting arc faults;

Fig. 23 is a schematic diagram of the monitoring/interrupting circuitry for the fault sensing circuitry of Fig. 22;

Fig. 24 is a schematic diagram of the processing circuitry for the fault sensing circuitry of Fig. 22;

Fig. 25 is schematic diagram of the monitoring/interrupting circuitry for a circuit breaker with combined fault detection capabilities, illustrating circuitry capable of monitoring ground faults and circuitry capable of monitoring arc faults;

Fig. 26 is a block diagram for the fault sensing circuitry for detecting multiple types of faults;

Fig. 27 is schematic diagram of the monitoring/interrupting circuitry for a circuit breaker with combined fault detection capabilities, illustrating circuitry capable of

monitoring ground faults and circuitry capable of monitoring arc faults at both the line side and the load side;

Fig. 28 is a schematic diagram of the processing circuitry for detecting arc faults on the line side of the fault sensing circuitry of Fig. 26;

Fig. 29 is a schematic diagram of the processing circuitry for detecting arc faults on the load side of the fault sensing circuitry of Fig. 26;

Fig. 30 is a schematic diagram for the arc fault trigger generator for the fault sensing circuitry of Fig. 26;

Fig. 31 is a schematic diagram of an alternative embodiment for the SCR trigger circuit; and

Fig. 32 is a block diagram of an exemplary circuit interrupting system for home power distribution system incorporating a GFCI circuit breaker having a reset lockout operation according to the present application.

DETAILED DESCRIPTION

Resettable Circuit Interrupting Devices

The present application relates to a family of resettable circuit interrupting devices for breaking and making electrical connections between input and output conductive paths associated with the devices and to systems incorporating such devices. The family of devices include: ground fault circuit interrupters (GFCI's), arc fault circuit interrupters (AFCI's), immersion detection circuit interrupters (IDCI's), appliance leakage circuit interrupters (ALCI's) and equipment leakage circuit interrupters (ELCI's). Generally, each circuit interrupting device according to the present application has a circuit interrupting portion, a reset portion and reset lockout portion, and an optional trip portion, which will be described in more detail below.

The circuit interrupting and reset portions preferably use electro-mechanical components to break and make the conductive path between input and output conductors. More particularly, the circuit interrupting portion is used to break electrical continuity between input and output conductive paths (or conductors) upon the detection of a fault. Operation of the reset and reset lockout portions is in conjunction with the operation of the circuit interrupting portion, so that the electrical connection between conductive paths cannot be reset if the circuit interrupting portion is non-operational and/or if an open neutral condition exists.

The trip portion preferably operates independently of the circuit interrupting portion so that in the event the circuit interrupting portion becomes non-operational the device can still be tripped. Preferably, the trip portion is manually activated and uses mechanical components to break the electrical connections. However, the trip portion may use electrical circuitry and/or electro-mechanical components to break the electrical connections.

For the purpose of the present application, the structure or mechanisms, used in the circuit interrupting devices, shown in the drawings and described hereinbelow are incorporated into GFCI receptacles suitable for installation in a single-gang junction box in a home, and GFCI circuit breakers suitable for installation in a circuit breaker panel.

However, the mechanisms according to the present application can be included in any of the various devices in the family of resettable circuit interrupting devices.

Turning now to Fig. 1, an exemplary GFCI receptacle is shown. The GFCI receptacle 10 has a housing 12 consisting of a relatively central body 14 to which a face or cover portion 16 and a rear portion 18 are removably secured. The face portion 16 has entry ports 20 for receiving normal or polarized prongs of a male plug of the type normally found at the end of a lamp or appliance cord set (not shown), as well as ground-prong-receiving openings 22 to accommodate a three-wire plug. The receptacle also includes a mounting strap 24 used to fasten the receptacle to a junction box.

A trip actuator 26, preferably a button, which is part of the trip portion to be described in more detail below, extends through opening 28 in the face portion 16 of the housing 12. The trip actuator is used, in this exemplary embodiment, to mechanically trip the GFCI receptacle, i.e., break the electrical connection between input and output conductive paths, independent of the operation of the circuit interrupting portion.

A reset actuator 30, preferably a button, which is part of the reset portion, extends through opening 32 in the face portion 16 of the housing 12. The reset button is used to activate the reset operation, which re-establishes electrical continuity between the input and output conductive paths, i.e., resets the device, if the circuit interrupting portion is operational.

Electrical connections to existing household electrical wiring are made via binding screws 34 and 36, where screw 34 is an input (or line) connection point and screw 36 is an output (or load) connection point. It should be noted that two additional binding screws (not shown) are located on the opposite side of the receptacle 10. Similar to binding screws 34 and 36, these additional binding screws provide input and output connection points. Further, the input connections are for line side phase (hot) and neutral conductors of the household wiring, and the output connections are for load side phase (hot) and neutral conductors of the household wiring. The plug connections are also considered output conductors. A more detailed description of a GFCI receptacle is provided in U.S. Patent 4,595,894 which is incorporated herein in its entirety by reference. It should also be noted that binding screws 34 and 36 are exemplary of the types of wiring terminals that

can be used to provide the electrical connections. Examples of other types of wiring terminals include set screws, pressure clamps, pressure plates, push-in type connections, pigtails and quick-connect tabs.

Referring to Fig. 2, the conductive path between the input connection point 34 and the output connection point 36 (or the entry ports 20) includes contact arm 70 which is movable between stressed and unstressed positions, movable contact 72, fixed contact 74 and contact arm 76. A movable latching member 60 and contacts 72 and 74 are used to make and break the conductive path.

There is also shown in Fig. 2, mechanical components used during circuit interrupting and device reset operations according to one embodiment of the present application. Although these components shown in the drawings are electro-mechanical in nature, the present application also contemplates using semiconductor type circuit interrupting and reset components, as well as other mechanisms capable or making and breaking electrical continuity.

The circuit interrupting portion has a circuit interrupter and electronic circuitry capable of sensing faults, e.g., current imbalances, on the hot and/or neutral conductors. In a preferred embodiment for the GFCI receptacle, the circuit interrupter includes a coil assembly 50, a plunger 52 responsive to the energizing and de-energizing of the coil assembly and a banger 54 connected to the plunger 52. The banger 54 has a pair of banger dogs 56 and 58 which interact with movable latching member 60 used to set and reset the connection between input and output conductors. The coil assembly 50 is activated in response to the sensing of a ground fault by, for example, the sense circuitry shown in Fig. 8. Fig. 8 shows conventional circuitry for detecting ground faults that includes a differential transformer that senses current imbalances.

The reset portion includes reset button 30, movable latching member 60 connected to the reset button 30, latching finger 64 and reset contacts 62 and 63 that temporarily activate the circuit interrupting portion when the reset button is depressed. Preferably, the reset contacts 62 and 63 are normally open momentary contacts. The latching finger 64 is used to engage side R of the contact arm 70 and move the arm 70 back to its stressed position where contact 72 touches contact 74.

The movable latching member 60 is, in this embodiment, common to each portion (i.e., the trip, circuit interrupting, reset and reset lockout portions) and used to facilitate making, breaking or locking out of the electrical connections between the input and output conductive paths. However, the circuit interrupting devices according to the present application also contemplate embodiments where there is no common mechanism or member between each portion or between certain portions.

In the embodiment shown in Fig. 2 and 3, the reset lockout portion includes latching finger 64 which after the device is tripped, engages side L of the movable arm 70 and blocks the movable arm 70 from moving so that contacts 72 and 74 are prevented from touching. In this embodiment, latching finger 64 acts as an active inhibitor that prevents the contacts from touching. Alternatively, the natural bias of movable arm 70 can be used as a passive inhibitor that prevents contacts 72 and 74 from touching.

Referring now to Figs. 2-4, the mechanical components of the circuit interrupter and reset mechanisms in various stages of operation are shown. In Fig. 2, the GFCI receptacle is shown in a set position where movable contact arm 70 is in a stressed condition so that movable contact 72 is in electrical engagement with fixed contact 74 of contact arm 76. If the sensing circuitry of the GFCI receptacle senses a ground fault, the coil assembly 50 is energized to draw plunger 52 into the coil assembly 50 so that banger 54 moves upwardly. As the banger moves upwardly, the banger front dog 58 strikes the latch member 60 causing it to pivot in a counterclockwise direction C about the joint created by the top edge 82 and inner surface 84 of finger 80. The movement of the latch member 60 removes the latching finger 64 from engagement with side R of the remote end 73 of the movable contact arm 70, and permits contact arm 70 to return to its pre-stressed condition opening contacts 72 and 74, seen in Fig 3. It should be noted that the description thus far has been in terms of a single latch member 60 and a single contact arm 70. However, there are preferably two sets of latch members 60 and contact arms 70: one set for the phase (or hot) conductors (line and load side); and the other set for the neutral conductors (line and load side). Further, the banger 54 preferably has two sets of banger dogs: one set for the phase conductors (line and load side); and the other set for the neutral conductors (line and load side).

After tripping, the coil assembly 50 is de-energized so that spring 53 returns plunger 52 to its original extended position and banger 54 moves to its original position releasing latch member 60. At this time the latch member 60 is in a lockout position where latch finger 64 inhibits movable contact 72 from engaging fixed contact 74, as seen in Fig. 6. As noted, latching finger 64 acts as an active inhibitor that prevents the contacts from touching. Alternatively, the natural bias of movable arm 70 can be used as a passive inhibitor that prevents contacts 72 and 74 from touching.

To reset the GFCI receptacle so that contacts 72 and 74 are closed and continuity between the input and output conductors is reestablished, the reset button 30 is depressed sufficiently to overcome the bias force of return spring 90 and move the latch member 60 in the direction of arrow A, seen in Fig. 4. While the reset button 30 is being depressed, latch finger 64 contacts side L of the movable contact arm 70 and continued depression of the reset button 30 forces the latch member to overcome the stress force exerted by the arm 70 causing the reset contact 62 on the arm 70 to close on reset contact 63. Closing the reset contacts activates the operation of the circuit interrupter by, for example simulating a fault, so that plunger 52 moves the banger 54 upwardly so that the banger dog 58 strikes the latch member 60 pivoting the latch member in the direction of arrow C while the latch member 60 continues to move in the direction of arrow A. As a result, the latch finger 64 is lifted over side L of the remote end 73 of the movable contact arm 70 onto side R of the remote end of the movable contact arm, as seen in Fig. 7. Contact arm 70 returns to its unstressed position opening contacts 62 and 63, so as to terminate the activation of the circuit interrupting portion, thereby de-energizing the coil assembly 50.

After the circuit interrupter operation is activated, the coil assembly 50 is de-energized so that so that plunger 52 returns to its original extended position, and banger 54 releases the latch member 60 so that the latch finger 64 is in a reset position, seen in Fig. 5. Release of the reset button causes the latching member 60 and movable contact arm 70 to move in the direction of arrow B until contact 72 electrically engages contact 74.

Referring again to Figs. 2 and 3 the trip portion according to this embodiment the present application includes a trip actuator 26, preferably a button, that is movable between a set position, where contacts 72 and 74 are permitted to close or make contact, as seen in

Fig. 2, and a trip position where contacts 72 and 74 are caused to open, as seen in Fig. 3. Spring 100 normally biases trip button 26 toward the set position. The trip portion also includes a trip arm 102 that extends from the trip button 26 so that a surface 104 of the trip arm 102 moves into contact with the movable latching member 60, when the trip button is moved toward the trip position. When the trip button 26 is in the set position, surface 104 of trip arm 102 can be in contact with or close proximity to the movable latching member 60, as seen in Fig. 2.

In operation, upon depression of the trip button 26, the trip button pivots about point T of pivot arm 106 extending from strap 24 so that the surface 104 of the trip arm 102 can contact the movable latching member 60. As the trip button is moved toward the trip position, trip arm 102 also enters the path of movement of the finger 80 associated with reset button 30 thus blocking the finger 80 from further movement in the direction of arrow A. By blocking the movement of the finger 80, the trip arm 102 inhibits the activation of the reset operation and, thus, inhibits simultaneous activation of the trip and reset operations. Further depression of the trip button 26 causes the movable latching member 60 to pivot about point P (Fig. 3) in the direction of arrow C. Pivotal movement of the latching member 60 causes latching finger 64 to move out of contact with the movable contact arm 70 so that the arm 70 returns to its unstressed condition, and the conductive path is broken. Resetting of the device is achieved as described above.

An alternative embodiment of the trip portion will be described with reference to Figs. 9 and 10. In this embodiment, the trip portion includes a trip button 26 that is movable between a set position, where contacts 72 and 74 are permitted to close or make contact, as seen in Fig. 9, and a trip position where contacts 72 and 74 are caused to open, as seen in Fig. 10. Spring 110 normally biases trip button 26 toward the set position. The trip portion also includes a trip arm 112 that extends from the trip button 26 so that a distal end 114 of the trip arm is in movable contact with the movable latching member 60. As noted above, the movable latching member 60 is, in this embodiment, common to the trip, circuit interrupting, reset and reset lockout portions and used to make, break or lockout the electrical connections between the input and output conductive paths.

In this embodiment, the movable latching member 60 includes a ramped portion 60a which facilitates opening and closing of electrical contacts 72 and 74 when the trip button 26 is moved between the set and trip positions, respectively. To illustrate, when the trip button 26 is in the set position, distal end 114 of trip arm 112 contacts the upper side of the ramped portion 60a, seen in Fig. 9. When the trip button 26 is depressed, the distal end 114 of the trip arm 112 moves along the ramp and pivots the latching member 60 about point P in the direction of arrow C causing latching fingers 64 of the latching member 60 to move out of contact with the movable contact arm 70 so that the arm 70 returns to its unstressed condition, and the conductive path is broken. Resetting of the device is achieved as described above.

Using the reset lockout feature described above permits the resetting of the GFCI device or any of the other devices in the family of circuit interrupting devices only if the circuit interrupting portion is operational. Thus, testing of the circuit interrupting portion occurs during the reset operation. Further, if the circuit interrupting portion becomes non-operational after the device is set, the independent trip mechanism can still trip the device. In other words, the circuit interrupting device according to the present application can be tripped whether or not the circuit interrupting portion is operating properly.

The circuit interrupting device according to the present application can be used in electrical systems, shown in the exemplary block diagram of Fig. 11. The system includes a source of power 120, such as ac power in a home, at least one circuit interrupting device 10 electrically connected to the power source, and one or more loads 122 connected to the circuit interrupting device. As an example of one such system, ac power supplied to single gang junction box in a home may be connected to a GFCI receptacle having the above described independent trip and reset lockout features, is installed in the junction box. Household appliances that are then plugged into the receptacle become the load or loads of the system.

Circuit Breakers

As noted above, various types of circuit interrupting devices are contemplated by the present application. The resettable receptacle with fault protection described above is

one example. Another example is a resettable circuit breaker with fault protection. Generally, such circuit breakers are used as resettable branch circuit protection devices, which are capable of opening a conductive path supplying electrical power to various loads in a power distribution system (or sub-system) if a fault occurs or if the current rating of the circuit breaker is exceeded. Such circuit breakers are also capable of being reset to close the conductive path. The conductive path is typically divided between a line side and a load side. Thus, the circuit breaker has line and load phase (or power) connections. The line side has a line phase connection and the load side has a load phase connection. The line phase connection connects to supplied power and the load phase connection connects to one or more loads. The connections are connection points where external conductors can be connected to the circuit breaker. These connections may be, for example, electrical fastening devices, such as binding screws, lugs or binding plates, that secure the external conductor to the circuit breaker, as well as conduct electricity.

As noted above, the circuit breakers according to the present application can provide fault protection for various types of faults or combination of faults. Examples of the various faults contemplated include ground faults, arc fault, immersion detection faults, appliance leakage faults and equipment leakage faults. Although many various types of fault protection circuit breakers are contemplated, the following descriptions are for GFCI circuit breakers and AFCI circuit breakers.

Ground Fault Circuit Interrupter Circuit Breakers

An exemplary embodiment of a GFCI circuit breaker incorporating a reset lockout will now be described. Generally, each GFCI circuit breaker according to the present application has a circuit interrupting portion, a reset portion and a reset lockout. The GFCI circuit breaker may also include a trip portion that operates independently of the circuit interrupting portion.

The circuit interrupting and reset portions preferably use electro-mechanical components to break (open) and make (close) the conductive path between the line and load phase connections. However, electrical components, such as solid state switches and supporting circuitry, may be used to open and close the conductive path. Similar to the

embodiments described above, the circuit interrupting portion is used to automatically break electrical continuity in the conductive path (i.e., open the conductive path) between the line and load phase connections upon the detection of a ground fault. The reset portion is used to disable the reset lockout and to permit the closing of the conductive path. That is, the reset portion permits re-establishing electrical continuity in the conductive path from the line connection to the load connection. Operation of the reset and reset lockout portions is in conjunction with the operation of the circuit interrupting portion, so that the electrically conductive path between the line and load phase connections cannot be reset if the circuit interrupting portion is non-operational and/or if an open neutral condition exists.

Circuit breakers with an independent trip portion can still be tripped, i.e., the conductive path between the line and load phase connections can still be opened, even if the circuit interrupting portion becomes non-operational. Preferably, the trip portion is manually activated and uses mechanical components to open the conductive path. However, the trip portion may use electrical components, such as solid state switches and supporting circuitry, and/or electro-mechanical components, such as relay switches, to open the conductive path between the line and load phase connections.

Referring now to Fig. 12, the GFCI circuit breaker 200 has a housing 210 configured for installation in conventional circuit breaker panels (not shown). Line and load power (phase) connections 212 and 214, and line and load neutral connections 216 and 218 are accessible from an exterior of the housing 210 and are provided for connecting the circuit breaker to external wiring. An actuator 220 extends through an exterior surface of the housing 210 and is used to manually set the operating condition or state of the circuit breaker. A trip actuator 222, which will be described in more detail below, extends through the exterior surface of the housing 210. The trip actuator 222 is used, in this exemplary embodiment, to mechanically trip the GFCI circuit breaker independent of the operation of the circuit interrupting portion.

Referring to Fig. 13, a power control assembly 224, which forms a portion of the conductive path, is used to make and break the conductive path. Generally, the power control assembly 224 operates similar to the operation of a toggle switch. In the exemplary embodiment shown in Figs. 13-18, the power control assembly 224 includes the actuator

220 which is movable between 'on', 'off' and 'trip' positions and a pair of electrical contacts 226 and 228 that are opened and closed depending upon the state the circuit breaker is in. Preferably, one of the contacts is fixed relative to the other. For example, in the embodiment shown in Fig. 13, fixed contact 226 is attached to or monolithically formed into the line power connection 212, and the movable contact 228 is attached to or monolithically formed into movable contact arm 230. However, the present application also contemplates circuit breaker configurations where each contact is movable relative to the other.

The movable contact arm 230 is pivotally connected to the actuator 220 such that movement of the actuator is translated to movement of the contact arm 230, or movement of the contact arm 230 is translated to movement of the actuator 220. Preferably, the contact arm 230 is movable between a closed position where contacts 226 and 228 are closed and the conductive path is completed (Fig. 13), and an open position where contacts 226 and 228 are open and the conductive path is broken (Fig. 14). When the contacts are closed, the circuit breaker 200 is in an 'on' state so that electricity can flow from the line connection to the load connection and the ground fault protection is armed. When the contacts are open, the circuit breaker 200 can be in either a 'tripped' state or an 'off' state. In the 'tripped' state, current cannot flow from the line connection to the load connection and the reset lockout is enabled. In the 'off' state current cannot flow from the line connection to the load connection but the reset lockout is not enabled.

A trip/reset assembly 240 is operatively coupled to the power control assembly 224 and is used for ground fault protection and resetting of the circuit breaker 200. In this embodiment, the trip/reset assembly operates as the above-described circuit interrupting portion and the reset portion. When the trip/reset assembly operates to provide fault protection, the assembly operates as the circuit interrupting portion. When the trip/reset assembly 240 operates to reset the circuit breaker, the assembly operates as the reset portion. The trip/reset assembly also provides the current protection for the circuit breaker 200. That is, if the current flowing from the line connection to the load connection exceeds a predetermined current rating for the circuit breaker (e.g., 15 amps), then the

trip/reset assembly will respond by causing the power control assembly 224 to open the conductive path, e.g., contacts 226 and 228 will open.

The trip/reset assembly 240 according to this exemplary embodiment includes mechanical linkage 242 to the power control assembly and sensing circuitry included on wiring board 244. The sensing circuitry, examples of which are shown in Figs. 19-21, is used to sense ground faults and is similar to the sensing circuitry shown in Fig. 8. However, other known circuits capable of detecting ground faults may also be utilized. The test/reset assembly mechanical linkage 242 includes control arm 246, latch arm 248 that is movably coupled to latch arm support 250, and latch arm controller 252. The control arm 246 is operatively coupled to the movable contact arm 230 via spring 254, so that if the actuator 220 is in the 'on' position (Fig. 13), the control arm catch 256 is releasably latched to the latch arm 248 to arm the ground fault protection, as seen in Fig. 13. Similarly, when the actuator 220 is in the 'off' position (Fig. 17) the control arm catch 256 is releasably latched to the latch arm 248, as seen in Fig. 17. When the actuator 220 is in the 'trip' position (Fig. 14), the control arm catch 256 disengages from the latch arm 248 and the reset lockout is enabled. It should be noted that in this embodiment, the control arm catch 256 also operates as the reset lockout which will be described in more detail below.

The latch arm controller 252 includes solenoid 258 and latch arm linkage 260 which couples the latch arm 248 to the solenoid piston 262 such that movement of the solenoid piston is translated to pivotal movement of the latch arm 248. The trip/reset assembly 240 also includes a reset enable switch assembly 270 that is activated by switch activator 264 secured to the latch arm 248. The reset enable switch assembly is provided to induce or simulate a ground fault condition on the sensing circuitry so that the circuit interrupting portion is activated to disable the reset lockout, as will be described in more detail below. As noted, the latch arm 248 is pivotally movable relative to the latch arm support 250. In addition, the latch arm is also movable in a direction parallel to the latch arm support 250 such that upward movement of the latch arm 248 causes the switch actuator 264 to move in a manner which activates the reset enable switch assembly 270 which, in turn, activates the circuit interrupting portion, if operational. If the circuit interrupting portion is not

operational, the circuit breaker cannot be reset. Various switching arrangements for the reset enable switch assembly 270 are shown in Figs. 19-21. For example, in Fig. 19, the reset enable switch assembly 270 includes a fixed contact 272, that may be a rigid wire strip, which induces and/or simulates a ground fault when the fixed contact 272 and the switch actuator 264 of the latch arm 248 come into contact. Simulating the ground fault causes the solenoid 258 to energize. The power for the circuit in Fig. 19 is supplied by the line side connection.

In Fig. 20, the reset enable switch assembly 270 includes a pair of momentary switches 274 and 276. In some circuit breaker designs power to the sensing circuitry is from the load side, so that when the circuit breaker trips power to the sensing circuit is turned off. In this embodiment, switch 276 is a normally closed momentary switch. When in the closed position, switch 276 powers the sensing circuitry from the load side of the breaker contacts and when activated during a reset operation, momentarily powers the sensing circuitry from the line side connection 212 and then returns to the normally closed position if the circuit breaker resets. Switch 274 is preferably configured so that it is opened when contacts 226, 228 are closed, and so that it is closed when the breaker contacts 226, 228 are opened. To avoid unintended simulated ground fault conditions, switch 274 opens before the circuit breaker contacts 226, 228 close, and switch 274 closes after the circuit breaker contacts 226, 228 open. This functions to introduce a simulated fault condition to the sensing circuitry. As the sensing circuitry is being powered from the load side and the breaker contacts are open the solenoid 258 is not activated. When a reset operation is being performed so that power is temporarily switched to the line side by switch 276, the solenoid is capable of being energized to permit resetting of the circuit breaker.

In Fig. 21, the reset enable switch assembly 270 includes a series of switch contacts 280, 282, 284, 286 and 288 which are sequentially activated or deactivated (depending upon their normal state) by pressure from the switch actuator 264 as the latch arm 248 moves in direction U (Fig. 15) when moving actuator 220 to the 'off' position. For example, initial motion of the switch actuator 264 breaks contact 280 from contact 282. Continued pressure causes contact 282 to close with contact 284. Further pressure causes

contact 286 to close with contact 288 which introduces a phase voltage to the sensing circuitry, thus, simulating a ground fault. It should be noted that in both embodiments, power is connected to the sensing circuitry from the load connection side when the circuit breaker 200 is in the 'on', 'off' or 'tripped' states, and power is supplied to the sensing circuitry from the line connection side while resetting the circuit breaker.

To prevent multiple firings of the solenoid, the reset enable switch assembly is preferably configured to induce and/or simulate the ground fault condition while in the lock-out condition until solenoid 258 trips latch arm 248 and releases control arm catch 256 or actuator 220 is released. Thus, in the embodiment of Fig. 19, the switch actuator 264 is positioned on the latch arm 248 so that when the reset lockout is disabled, the latch arm 248, and thus the switch actuator 264, move away from the reset enable switch assembly in response to the biasing force of spring 265, so that the switch becomes deactivated.

The portion of the trip/reset assembly used to perform the tripping operation is also designated as the circuit interrupting portion, and the portion of the trip/reset assembly used to perform the reset operation is also designated as the reset portion. Further, the portion of the trip/reset assembly used to perform current protection is also designated as the current protection portion.

Referring now to Figs. 14 and 15, the reset lockout inhibits the actuator 220 in the power control assembly 220 from moving from the 'tripped' position to the 'off' position so that the circuit breaker cannot be reset. In the embodiment shown in Figs. 14 and 15, the reset lockout operates as an active lockout in which the lockout actively inhibits (or prevents) the actuator 220 from moving from the 'tripped' position to the 'off' position. However, the reset lockout may also be configured to passively inhibit movement of the actuator 220 by, for example, the inherent operation of a spring. The reset lockout includes the control arm catch 256 attached to or formed into the control arm 246 so that when the actuator 220 is manually moved in the direction of arrow F, toward the 'off' position, the catch 256 engages surface 248a of the latch arm 248 which inhibits movement of the actuator 220.

In this embodiment, the conductive path extends from line power connection 212 to load power connection 214 via the power control assembly 224, the trip/reset assembly and

transformer assembly 290. The transformer assembly includes a differential transformer and ground/neutral coil shown in Figs. 19 and 20.

Typically, circuit breakers are reset by first moving the actuator 220 to the 'off' position and then moving the actuator to the 'on' position. While this sequence of movements of the actuator are being performed, the control arm 246 and latch arm 248 are moved so that the control arm catch 256 is releasably latched to the latch arm 248. The circuit breaker is in the 'on' state so that the conductive path is closed and ground fault protection is armed.

The operation of the circuit breaker 200 embodiment according to the present application will now be described with reference to Figs. 13-18. As noted, the actuator 220 is movable between 'on', 'off' and 'trip' positions, where the 'trip' position is typically between the 'on' and 'off' positions. To put the circuit breaker in the 'on' position (from the 'off' position, Fig. 17) the actuator 220 of the power control assembly 224 is moved in the direction of arrow O. When in the 'on' position (Fig.13), the conductive path between the line and load connections is closed, the control arm catch 256 is releasably latched to the latch arm 248, as seen in Fig. 13, and the reset enable switch assembly 270 is in its normal state. At this point the circuit breaker is in the 'on' state, where the ground fault protection is armed and the breaker is capable of tripping.

If a fault is detected by the sensing circuitry, the solenoid 258 is energized so that the solenoid piston 262 retracts, causing the latch arm linkage 260 to pull the latch arm 248 away from the control arm 246. Once the latch arm 248 moves far enough away from the control arm 246 the control arm catch 256 is released from the latch arm 248. After the catch 256 is released, the tension in spring 254 causes the control arm 246 to pivot in the direction of arrow P' permitting arm 230 to pivot in direction P causing contacts 226, 228 to open and the actuator 220 to automatically move to the 'trip' position, seen in Fig. 14. At this time, the circuit breaker is in the 'tripped' state.

When the circuit breaker is in the 'tripped' state, the reset lockout portion of the breaker is enabled, as seen in Fig. 14, so that the circuit breaker cannot be reset, unless the circuit interrupting portion is operational to disable the reset lockout. Fig. 15 shows the control arm catch 256 (i.e., the reset lockout) in a lockout position where catch 256 is

engaged with the surface 248a of the latch arm 248, thus preventing further movement of the actuator 220 toward the 'off' position.

To reset the circuit breaker, further movement of the actuator 220 in the direction of arrow F activates reset enable switch assembly 270 so that if the circuit interrupting portion is operational, the solenoid 258 will energize causing the latch arm linkage 260 and thus the latch arm 248 to retract. When the latch arm 248 retracts, the control arm catch 256 disengages from the latch arm 248 so that the actuator 220 is no longer inhibited from moving to the 'off' position, as seen in Fig. 17.

Referring again to Figs. 13 and 14 the trip portion according to this embodiment of the present application includes the trip actuator 222 and a trip arm 292. Preferably, the trip actuator 222 is a button that is movable between a set position, where contacts 226 and 228 are permitted to close (seen in Fig. 13) and a trip position where contacts 226 and 228 are caused to open (seen in Fig. 14). Spring 294 normally biases trip button 222 toward the set position. The trip arm 292 that extends from the trip button 222 so that a surface 296 of the trip arm 292 can move into contact with the control arm 246 when the trip button 222 is moved toward the trip position (i.e., when the trip button is depressed).

To trip the circuit breaker 200 independently of the operation of the circuit interrupting portion, the trip actuator 222 is depressed so that surface 296 of trip arm 292 pushes against the control arm 246 and surface 309 of trip arm 292 pushes against latch arm 248 causing the control arm catch 256 to release from the latch arm 248. The tension in spring 254 causes the contact arm 246 and thus contact 228 to pivot away from the fixed contact 226, thus opening the conductive path.

Arc Fault Circuit Interrupter Circuit Breakers

An exemplary embodiment of an AFCI circuit breaker incorporating a reset lockout will now be described. Generally, each AFCI circuit breaker according to the present application has a circuit interrupting portion, a reset portion and a reset lockout. Similar to the GFCI circuit breaker, the circuit interrupting and reset portions preferably use electro-mechanical components to break (open) and make (close) the conductive path between the line and load phase connections. However, electrical components, such as solid state

switches and supporting circuitry, may be used to open and close the conductive path. Similar to the embodiments described above, the circuit interrupting portion is used to automatically break electrical continuity in the conductive path (i.e., open the conductive path) between the line and load phase connections upon the detection of an arc fault. The reset portion is used to disable the reset lockout and to permit the closing of the conductive path. That is, the reset portion permits re-establishing electrical continuity in the conductive path from the line side connection to the load side connection. Operation of the reset and reset lockout portions is in conjunction with the operation of the circuit interrupting portion so that the electrically conductive path between the line and load phase connections cannot be reset if the circuit interrupting portion is non-operational and/or if an open neutral condition exists.

Similar to the GFCI circuit breaker, the AFCI circuit breaker may also include a trip portion that operates independently of the circuit interrupting portion. AFCI circuit breakers with this trip portion can still be tripped, i.e., the conductive path between the line and load phase connections can still be opened, even if the circuit interrupting portion becomes non-operational. Preferably, the trip portion is manually activated and uses mechanical components to open the conductive path. However, the trip portion may use electrical components, such as solid state switches and supporting circuitry, and/or electro-mechanical components, such as relay switches and supporting circuitry, to open the conductive path between the line and load phase connections.

The circuit interrupting, reset, reset lockout and optional trip portions according to this embodiment are substantially the same as those for the above-described GFCI circuit breaker embodiment. These portions are shown in Figs. 12-18 and for simplicity the descriptions of these portions are not repeated. A difference between the GFCI and the AFCI circuit breakers is the sensing circuitry used to detect faults. Figs. 22-24 show one exemplary embodiment of the sensing circuitry that can be used to detect arc faults. However, a more detailed description of the arc fault sensing circuitry can be found in commonly owned, co-pending application Serial No. 08/994,772, filed December 19, 1997 which is incorporated herein in its entirety by reference. In addition, alternative techniques

for sensing arc faults are provided in commonly owned, copending applications Serial Nos. 08/993,745 and 08/995,130 both of which are incorporated herein by reference.

Generally, the sensing circuitry can be configured to monitor the phase conductive path 410 (Fig. 22) at either the line side of the conductive path, the load side of the conductive path or at both the line and load sides of the conductive path. The sensing circuitry can also be configured to implement many of the various techniques capable of monitoring one or more conductive paths and determining whether signals on a conductive path comprise an arc fault. Similar to the above described GFCI circuit breaker embodiment, the sensing circuitry also operates to interrupt the AC power on at least the phase conductive path by opening contacts 226 and 228 (Seen in Fig. 13) via the actuation of solenoid 258.

In the embodiment of Fig. 22, the conductive path 410 extends from line power connection 212 to load power connection 214 via the power control assembly 224, the trip/reset assembly 240 and transformer assembly 430.

The following is a description of an exemplary embodiment of the sensing circuitry contemplated by the present application. Referring to Fig. 22, the sensing circuitry includes a path control portion 411, a pickup portion 412 and a processing portion 414. The path control portion 411 provides power to the circuitry used to detect arc faults and to the components used to open the conductive path if an arc fault is detected. The pickup portion 412 monitors the conductive path 410 and picks up spurious signals from the conductive path, which may include arc faults. The processing portion 414 receives the arcing signals and 1) determines whether the arcing signals include an arc fault, and 2) provides a trigger signal to open the conductive path if an arc fault is detected.

Referring to Fig. 23 an exemplary schematic diagram for the path control and pickup portions 411 and 412 is shown. In this embodiment, the path control portion 411 includes a power supply circuit 418 connected to the line phase and neutral connections 212 and 216 respectively, and an SCR 422 that selectively energizes solenoid 258. The power supply also provides power, typically 26 volts, to the processing circuitry through voltage dropping resistor 417 and capacitor 419, shown in Fig. 23. Capacitor 423 prevents voltage spikes on the line from causing the SCR 422 to inadvertently trigger, and resistor 425

prevents the gate of the SCR 422 from floating and ensures that the SCR turns off when the TRIG_AFCI signal (described below) goes away. Resistor 427 is used to drop the voltage from the TRIG_AFCI signal to a level suitable for the SCR 422.

The pickup portion 412 includes transformer assembly 430 which picks up spurious signals, which may include arc faults, on the conductive path 410. However, the spurious signals can also be detected using capacitive coupling via capacitors coupled to the conductive path 410. Techniques of using capacitive coupling onto the AC line to detect spurious voltage signals are known and can be used instead of the transformer assembly 430. The transformer assembly 430 includes a magnetic core 431 and a coil 432 constructed using, for example, known toroidal ferrite design techniques. Preferably, the ferrite material and the turn ratio of the magnetic core 431 and coil 432 are chosen to achieve a natural resonance at about 1.5 MHz. A resistor 434 in combination with capacitor 436 form a resonance damping network for broadband frequency pickup. This configuration enables the sensing circuitry to react to a wider range of spurious signals from different sources rather than limiting the sensing circuitry to detecting signals within a limited frequency spectrum.

The signal generated by transformer assembly 430 is transferred to capacitor 438 which performs a DC decoupling function, and diodes 440, 442 prevent low level signals below about 0.6 V peak to peak from entering the processing circuitry. The signal output by the pickup portion 412 is identified as an arcing signal, labeled ARC_SENSE, and is transferred to the processing portion 414. As noted, the processing portion determines whether the spurious signal, ARC_SENSE, includes characteristics that qualify as an arc fault.

A schematic diagram illustrating the processing circuitry 414 is shown in Fig. 24. The processing circuit 414 includes an amplifier 450, a filter 452, a rectifier 454, and a peak detector 456.

The amplifier 450 includes a resistor divider network that includes resistors 458 and 460 which determine the maximum dynamic range of the amplifier 450. The amplifier 450 also includes an operational amplifier (op amp) 462 having a fixed gain provided by resistors 464 and 466. The plus input of the op amp 462 is tied to ground

potential by resistor 468, and the minus input to the op amp 462 is connected to the junction of resistors 464 and 466, as shown in Fig. 24.

The output of the op amp 462 is input to frequency selective circuitry, such as filter 452. Preferably, the filter 452 is a 2nd order Butterworth high pass active filter, which provides better cut off response than passive filters. However, passive type filter designs, such as LC filters, can also be used. The filter 452 includes an op amp 470 connected to an RC network including capacitors 472, 474 and resistors 476, 478, 480, which perform the filtering function. Utilizing capacitors and resistors in conjunction with the op amp 470 provides a steeper roll off in frequency gain below 500 KHz than would be achieved with passive components alone. Preferably, the internal operating characteristics of the op amp 470 provide the upper limit to the high frequencies passed by the filter 452. To permit maximum utilization of the high frequency characteristics of the op amp 470, the gain of the op amp is preferably set at unity. Filter 452 permits the detection of arc faults even if the AC power lines (including the conductive path) are being used for data communications which typically occur at frequencies below 500 KHz.

The output of the filter 452 is input to the rectifier 454 which is preferably a full wave rectifier. The rectifier 454 includes an op amp 482 having its plus input connected to ground and its minus input connected to its feedback path. The rectifier 454 provides a variable level of gain, depending on whether the input signal from the filter 452 is positive or negative. To illustrate, for positive input signals the gain is zero and for negative signals the gain is determined by the ratio of resistors 484 and 486. If the input signal is positive relative to ground, the output of the op amp 482 is negative which pulls the minus input of the op amp down through diode 488 until it is equal to the plus input. Thus, the amplifier has a gain of zero. If, on the other hand, the signal input to the minus input is negative relative to ground, the output of the op amp 482 is positive and feedback current flows through diode 490 and resistor 486.

The signal output from the rectifier 454 is in the form of a pulsed DC voltage, which is fed to the peak detector 456. The peak detector 456 has a constant current source that includes op amp 492, diode 494 and resistors 496, 498 and 499. The constant current source is responsive to the pulsed DC voltage from the rectifier 454, and provides a linear

charging curve across capacitor 500. The rate of charging of the capacitor 500 is proportional to the number of positive signals input to the peak detector from the rectifier 454.

As shown in Fig. 24, capacitor 500 is continually being discharged through resistor 502. In addition, the peak detector 456 functions as an integrator and a time delay circuit which aids in preventing the circuit from reacting to acceptable short lived arcing spikes created when, for example, a switch is thrown or an appliance is plugged in.

The arcing signals being detected by the processing circuitry 414 can be categorized into three main types: high, low and very low arcing signals. In the presence of a high arcing signal, the output of the rectifier 454 includes a substantial number of DC pulses so that the current output by the constant current source rapidly charges the capacitor 500 causing the voltage across the capacitor to reach a zener diode breakdown voltage of output transistor 504 relatively quickly.

When the signal detected is a low arcing signal, the peak detector 456 generates pulses that are more dispersed, causing the voltage across capacitor 500 to rise more slowly, thus delaying the breakover of the zener diode breakdown voltage of transistor 504. In this instance, although resistor 502 continuously discharges the capacitor 500, if the pulses from the rectifier 454 continue for a sufficient enough time to completely charge the capacitor 500, breakover of the zener diode breakdown voltage of transistor 504 can occur.

When the signal detected is a very low arcing signal, the discharge rate of the capacitor 500 via resistor 502 is greater than or equal to the charging rate of the capacitor 500. Thus, the voltage across the capacitor 500 does not reach a sufficiently high level to cause breakover of the zener diode breakdown voltage of transistor 504.

The output of transistor 504, labeled TRIG_AFCI, is the trigger signal for the SCR 422 (seen in Fig. 23). Thus, the TRIG_AFCI signal is input to the gate of the SCR 422 through resistor 427 which turns on the SCR and thus energizes the solenoid 258. As described above, energization of the solenoid 258 causes the contacts 226 and 228 to open or permits resetting of the circuit breaker. The solenoid 258 is de-energized after the gate signal is removed and the rectified AC decreases to a level close to zero. As noted, resistor 425 ensures that the gate of the SCR 422 turns off when there is no TRIG_AFCI

signal. It should be noted that if an arc is upstream from the circuit breaker, opening the contacts stops the pickup portion from picking up spurious signals (including the arc). If the arc is downstream from the circuit breaker, opening the contacts extinguishes the arc and, thus, removes the TRIG_AFCI signal.

The operation of the AFCI circuit breaker is similar to the operation of the GFCI circuit breaker described above with reference to Figs. 13-18. In operation, the actuator 220 is movable between 'on', 'off' and 'trip' positions, where the 'trip' position is typically between the 'on' and 'off' positions. To put the circuit breaker in the 'on' position (from the 'off' position, Fig. 17) the actuator 220 of the power control assembly 224 is moved in the direction of arrow O. When in the 'on' position (Fig.13), the conductive path between the line and load connections is closed, the control arm catch 256 is releasably latched to the latch arm 248, as seen in Fig. 13, and the reset enable switch assembly 270 is in its normal state. At this point the circuit breaker is in the 'on' state, where the arc fault protection is armed and the breaker is capable of tripping.

If an arc fault is detected by the sensing circuitry described above for Figs. 22-24, the solenoid 258 is energized so that the solenoid piston 262 retracts, causing the latch arm linkage 260 to pull the latch arm 248 away from the control arm 246. Once the latch arm 248 moves far enough away from the control arm 246 the control arm catch 256 is released from the latch arm 248. After the catch 256 is released, the tension in spring 254 causes the control arm 246 to pivot in the direction of arrow P permitting arm 230 to pivot in a direction P' causing contacts 226, 228 to open and the actuator 220 to automatically move to the 'trip' position, seen in Fig. 14. At this time, the circuit breaker is in the 'tripped' state.

When the circuit breaker is in the 'tripped' state, the reset lockout portion of the breaker is enabled, as seen in Fig. 14, so that the circuit breaker cannot be reset, unless the circuit interrupting portion is operational to disable the reset lockout. Fig. 15 shows the control arm catch 256 (i.e., the reset lockout) in a lockout position where catch 256 is engaged with the surface 248a of the latch arm 248, thus preventing further movement of the actuator 220 toward the 'off' position.

To reset the circuit breaker, further movement of the actuator 220 in the direction of arrow F activates reset enable switch assembly 270 by closing switch 271, which is preferably a momentary switch. Closing switch 271 triggers pulse generator 273 which outputs a pulse that turns on oscillator 275 for a finite period of time at a resonant frequency of about 1.5 MHz. An example of a suitable pulse is a 10 ms pulse at low current, e.g., in the order of about 1-10 mA. If the circuit interrupting portion is operational, activation of the reset enable switch assembly 270, which simulates a fault, energizes the solenoid 258 causing the latch arm linkage 260 and thus the latch arm 248 to retract. When the latch arm 248 retracts, the control arm catch 256 disengages from the latch arm 248 so that the actuator 220 is no longer inhibited from moving to the 'off' position, as seen in Fig. 17.

Circuit Breakers With Combined Fault Detection Capabilities

The present application also contemplates circuit breakers that incorporate fault protection capabilities for more than one type of fault. For example, the circuit breaker can be configured with ground fault and arc fault protection, or the circuit breaker can be configured with ground fault and immersion detection fault protection. The construction of such circuit breakers can be similar to that shown in Figs. 12-18 and for simplicity is not repeated. That is, such circuit breakers would include a circuit interrupting portion, a reset portion, a reset lockout portion and, optionally, an independent trip portion. A difference in such combined fault protection circuit breakers would be in the sensing circuitry used to detect faults. The block diagram of Fig. 22 in combination with the schematic diagram of Fig. 25 show the sensing circuitry for one embodiment for a circuit breaker having ground fault and arc fault protection capabilities. Figs. 26-30 show sensing circuitry for another embodiment for a circuit breaker having ground fault and arc fault protection capabilities. These embodiments are exemplary. The present application contemplates circuit breakers with any number of fault protection capabilities in any combination.

The following description of Fig. 25 is an exemplary embodiment of sensing circuitry suitable for use in a circuit breaker with combined fault protection capabilities. In this embodiment, the conductive path 410 extends from line power connection 212 to load

power connection 214 via the power control assembly 224 (seen in Fig. 13), the trip/reset assembly 240 (seen in Fig. 13), transformer assembly 550 and transformer assembly 552. Generally, the sensing circuitry includes a path control portion 411, a pickup portion 412 and a processing portion 414 (seen in Fig. 24) similar to the embodiment of Fig. 22. The path control portion 411 provides power to the circuitry used to detect ground faults and arc faults, and to the components used to open the conductive path if a ground fault or an arc fault is detected. The pickup portion 412 monitors the conductive path 410 and picks up 1) ground faults and grounded neutral faults, and 2) spurious signals from the conductive path which may include arc faults. The processing portion 414 (seen in Fig. 24) receives arcing signals from the pick up portion and 1) determines whether the spurious signals include an arc fault, and 2) provides a trigger signal to open the conductive path if an arc fault is detected. In this embodiment, the processing portion 414 is the same as the processing portion 414 described above with reference to Fig. 24 and is not repeated.

Referring again to Fig. 25, the path control portion 411 includes a power supply circuit 560 connected to the line phase and neutral connections 212 and 216 respectively, SCR 562 and SCR trigger circuit 564. The power supply provides power, typically rectified AC, to the SCR 562, and provides power, typically 26 volts, to the components in the pickup and processing portions 412 and 414, and to the GFCI portion. The solenoid 258 is selectively energized in response to the output of SCR trigger circuit 564, which results in the opening and/or closing of contacts 226 and 228. Preferably, the SCR trigger circuit 564 performs an OR function so that either a ground fault or an arc fault trigger signal triggers the SCR 562.

The pickup portion 412 includes a ground fault pickup and an arc fault pickup. The ground fault pick up includes transformer assembly 550 having a differential transformer 570 and a ground neutral transformer 572 both coupled to an integrated circuit 580. The integrated circuit 580 is used to detect ground faults and to output a trigger signal, labeled TRIG_GFCI, to the SCR trigger circuit 564. Examples of suitable integrated circuits include the National Semiconductor LM1851 and the Raytheon RA9031. As noted above, such ground fault sensing circuitry is known.

The arc fault pickup includes transformer assembly 552 which picks up spurious current signals, which may include arc faults, on the conductive path. However, spurious voltage signals can also be detected using capacitive coupling via capacitors coupled to the phase conductive path. Techniques of using capacitive coupling onto the AC line are known.

The transformer assembly 552 has a magnetic core 590 and a coil 592 constructed using, for example, known toroidal ferrite design techniques. Preferably, the ferrite material and the turn ratio of the magnetic core 590 and coil 592 are chosen to achieve a natural resonance at about 1.5 MHz. A resistor 594 in combination with capacitor 596 forms a resonance damping network for broadband frequency pickup. This configuration of the arc fault pickup enables the sensing circuitry to react to a wider range of spurious signals from different sources rather than limiting the sensing circuitry to detecting signals within a limited frequency spectrum.

The signal generated by transformer assembly 552 is transferred to capacitor 598 which performs a DC decoupling function, and diodes 600, 602 prevent low level signals below about 0.6 V peak to peak from entering the processing circuitry 414. The signal output by the pickup portion is identified as an arcing signal, labeled ARC_SENSE, and is transferred to the processing portion 414. As noted, the processing portion determines whether the spurious signal includes characteristics that qualify it as an arc fault.

The operation of the circuit breaker with combined fault protection capabilities according to the embodiment of Figs. 22 and 25 is similar to the operation of the GFCI and AFCI circuit breakers described above with reference to Figs. 13-24, except that it is responsive to the detection of one or more types of faults.

In operation, the actuator 220 (seen in Fig. 17) is movable between 'on', 'off' and 'trip' positions, where the 'trip' position is typically between the 'on' and 'off' positions. To put the circuit breaker in the 'on' position (from the 'off' position, Fig. 17) the actuator 220 of the power control assembly 224 is moved in the direction of arrow O. When in the 'on' position (Fig.13), the conductive path between the line and load connections is closed, the control arm catch 256 is releasably latched to the latch arm 248, as seen in Fig. 13, and

the reset enable switch assembly 270 is in its normal state. At this point the circuit breaker is in the 'on' state, where fault protection is armed and the breaker is capable of tripping.

If a fault (e.g., an arc fault or a ground fault) is detected by the sensing circuitry described above for Figs. 22 and 25, the solenoid 258 is energized so that the solenoid piston 262 retracts, causing the latch arm linkage 260 to pull the latch arm 248 away from the control arm 246. Once the latch arm 248 moves far enough away from the control arm 246 the control arm catch 256 is released from the latch arm 248. After the catch 256 is released, the tension in spring 254 causes the control arm 246 to pivot in the direction of arrow P' permitting arm 230 to pivot in a direction P causing contacts 226, 228 to open and the actuator 220 to automatically move to the 'trip' position, seen in Fig. 14. At this time, the circuit breaker is in the 'tripped' state.

When the circuit breaker is in the 'tripped' state, the reset lockout portion of the breaker is enabled, as seen in Fig. 14, so that the circuit breaker cannot be reset, unless the circuit interrupting portion is operational to disable the reset lockout. Fig. 15 shows the control arm catch 256 (i.e., the reset lockout) in a lockout position where catch 256 is engaged with the surface 248a of the latch arm 248, thus preventing further movement of the actuator 220 toward the 'off' position.

To reset the circuit breaker, further movement of the actuator 220 (seen in Fig. 16) in the direction of arrow F activates reset enable switch assembly 270 (seen in Fig. 25) by closing switch 271, which is preferably a momentary switch. Closing switch 271 triggers pulse generator 273 which outputs a pulse that turns on oscillator 275 for a finite period of time at a resonant frequency of about 1.5 MHz. An example of a suitable pulse is a 10 ms pulse at a low current, e.g., in the order of about 1-10 mA. If the circuit interrupting portion is operational, activation of the reset enable switch assembly 270, which simulates a fault, energizes the solenoid 258 causing the latch arm linkage 260 and thus the latch arm 248 to retract. When the latch arm 248 retracts, the control arm catch 256 disengages from the latch arm 248 so that the actuator 220 is no longer inhibited from moving to the 'off' position, as seen in Fig. 17.

It should be noted that in the embodiment of Fig. 25, the GFCI portion is not activated for reset. However, it may be desirable to activate test circuits for both the GFCI and AFCI portions of the device, so that when resetting the device, both portions are tested before the device is reset. A description of this embodiment is described within the embodiment below.

It may be desirable for the sensing circuitry to generally pinpoint the location of an arc fault within a branch circuit. To accomplish this, a second arc fault pickup is added to the pickup portion 412, shown in Fig. 25, so that the pickup portion 412 outputs two separate arcing signals representing arcing signals picked up on the line and load sides. This embodiment of the sensing circuitry is shown in Figs. 26-30.

In this embodiment, the AC line (i.e., the line phase and neutral conductive paths) is partitioned into two different segments separated by the ground fault pickup of the pickup portion 412. The AC line is split for high frequency signals while the normal 50 or 60 Hz power transmission is unaffected. Referring to Fig. 27, the line and load arc fault pickups are, preferably, separated by the transformer assemblies 570 and 572 and ferrite transformers or beads 604 and 606 located on each side of the transformer assemblies. The ferrite transformers function to enhance the impedance of the AC line to high frequency signals.

The line side arc fault pickup includes transformer assembly 610 having a magnetic core 612 and a coil 614. The magnetic core 612 and coil 614 are constructed using, for example, known toroidal ferrite design techniques. Preferably, the ferrite material and the turn ratio of the magnetic core 612 and coil 614 are chosen to achieve a natural resonance at about 1.5 MHz. A resistor 616 in combination with capacitor 618 form a resonance damping network for broadband frequency pickup. This configuration enables the sensing circuitry to react to a wider range of spurious signals from different sources rather than limiting the sensing circuitry to detecting signals within a limited frequency spectrum. The load side pickup is the same as the arc fault pickup described above with reference to Fig. 25 and for simplicity is not repeated.

Similar to the above-described embodiments, the arcing signal can also be detected using capacitive coupling via capacitors on both the line side pickup and the load side pickup. Techniques of using capacitive coupling onto the AC line are known.

Schematic diagrams illustrating the line processing circuitry 414a and the load processing circuitry 414b are shown in Figs. 28 and 29, respectively. In this embodiment each processing circuit includes four processing stages; an AGC amplifier, a filter, a rectifier and a peak detector.

Referring to Fig. 28, in the line processing circuitry 414a, the LINE_ARC_SENSE signal is fed into the AGC amplifier 620, which includes a first resistor divider network having resistors 630, 632 and 634 that determine the maximum dynamic range of the AGC amplifier 620. Feedback control is provided through field effect transistor (FET) 636, which acts as a variable resistance in parallel with resistor 632. A second resistor divider network that includes resistors 638 and 640 provides a voltage level for the gate of FET 636. Preferably, a feedback signal, labeled LINE_AGC, input to FET 636 is proportional to a signal level developed on the load side. Similarly, a feedback signal, labeled LOAD_AGC, fed back to the AGC amplifier in the load circuitry (described hereinbelow in connection with Fig. 29) is preferably proportional to the signal level developed on the line side. This configuration provides additional differentiation between the line side and load side arcing signals sensed by the arc fault pickup.

The AGC amplifier 620 also includes an operational amplifier (op amp) 642 having a fixed gain provided by resistors 644 and 646. Resistor 644 is preferably a variable resistor that permits matching of the base gain of the AGC amplifier in both the line processing circuitry 414a and the load processing circuitry 414b. The plus input of the op amp 642 is connected to ground by resistor 648, and the minus input of the op amp is connected to resistors 644 and 646 as shown. To illustrate the effect of the feedback of the FET 636, assume that resistors 630, 632 and 634 are equal. With no feedback on the LINE_AGC signal, FET 636 is an open circuit and 67% of the LINE_ARC_SENSE signal enters op-amp 642. With full feedback on the LINE_AGC, the FET 636 is saturated so that only 50% of the LINE_ARC_SENSE signal enters the op-amp 642. By altering the

values of resistors 630, 632 and 634 and resistors 638 and 640, the weight and responsiveness of the AGC amplifier can be varied.

The output of the op amp 642 is input to frequency selective circuitry, such as filter 622. Preferably, the filter 622 is a 2nd order Butterworth high pass active filter, which provides better cut off response than passive filters. However, passive type filter designs, such as LC filters, can also be used.

Preferably, the filter 622 includes an op amp 650 connected to an RC network including capacitors 652, 654 and resistors 656, 658, 660 which perform the filtering function. Utilizing capacitors and resistors in conjunction with the op amp 650 provides a steeper roll off in frequency gain below 500 KHz than would typically be achieved with passive components alone. Preferably, the internal operating characteristics of the op amp 650 provide the upper limit to the high frequencies passed by the filter 622. To permit maximum utilization of the high frequency characteristics of the op amp 650, the gain of the op amp is preferably set at unity. Filter 622 permits the detection of arc faults even if the AC power lines (including the conductive path) are being used for data communications which typically occur at frequencies below 500 KHz.

The output of the filter 622 is input to the rectifier 624, which is preferably a full wave rectifier. Preferably, the rectifier 624 is configured to rectify input voltages in the millivolt range, and to provide a DC voltage for the peak detectors 626. The rectifier 624 includes an op amp 670 having its plus input connected to ground and its minus input connected to its feedback path. The rectifier 624 provides a variable level of gain, depending on whether the input signal from the filter 622 is positive or negative. To illustrate, for positive input signals the gain is zero, and for negative signals the gain is preferably determined by the ratio of resistors 672 and 674. If the input signal is positive relative to ground, the output of the op amp 670 is negative which pulls the minus input of the op amp down through diode 676 until it is equal to the plus input. Thus, the op amp 670 has a gain of zero. If, on the other hand, the signal input to the minus input is negative relative to ground, the output of the op amp 674 is positive and feedback current flows through diode 678 and resistor 674 and the gain is set by resistors 672 and 674.

The signal output from the rectifier 624 is in the form of a pulsed DC voltage, which is fed to the peak detector 626. The peak detector 626 has a constant current source that includes op amp 680, diode 682 and resistors 684,686 and 688. The constant current source is responsive to the pulsed DC voltage from the rectifier 624 and provides a linear charging curve across capacitor 690. The rate of charging of the capacitor 690 is proportional to the number of positive signals input to the peak detector 626 from the rectifier 624.

As shown in Fig. 28, capacitor 690 is continually being discharged through resistor 692. In addition, the peak detector 626 functions as an integrator and a time delay circuit which aids in preventing the circuit from reacting to acceptable short lived arcing spikes created when, for example, a switch is thrown or an appliance is plugged in.

The arcing signals being detected by the processing circuitry 414a can be categorized into three main types: high, low and very low arcing signals. In the presence of a high arcing signal, the output of the rectifier 624 includes a substantial number of DC pulses so that the current output by the constant current source rapidly charges the capacitor 690 causing the voltage across the capacitor 690 to reach a zener diode breakdown voltage of output transistor 694 relatively quickly.

When the signal detected is a low arcing signal, the peak detector 626 generates pulses that are more dispersed, causing the voltage across capacitor 690 to rise more slowly, thus delaying the breakover of the zener diode breakdown voltage of transistor 694. In this instance, although resistor 692 continuously discharges the capacitor 690, if the pulses from the rectifier 624 continue for a sufficient enough time to completely charge the capacitor 690, breakover of the zener diode breakdown voltage of transistor 694 can occur.

When the signal detected is a very low arcing signal, the discharge rate of the capacitor 690 via resistor 692 is greater than or equal to the charging rate of the capacitor 690. Thus, the voltage across the capacitor 690 does not reach a sufficiently high level to cause breakover of the zener diode breakdown voltage of transistor 694.

The output of transistor 694, labeled LINE_OUT, is input to arc fault trigger generator 700 (seen in Fig. 30), which as described below provides the trigger signal for the SCR 562 causing the solenoid 258 to be energized and contacts 226 and 228 to open or

permits resetting of the circuit breaker. Further, the output voltage of peak detector 626, designated LOAD_AGC, is used as the feedback signal for the AGC amplifier in the load processing circuitry 414b.

Referring now to Fig. 29 the load processing circuitry 414b is shown. In the load processing circuitry, the LOAD_ARC_SENSE signal is fed into an AGC amplifier 710 having a first resistor divider network that includes resistors 712, 714 and 716, and determines the maximum dynamic range of the AGC amplifier 710. Feedback control is provided through field effect transistor (FET) 718, which acts as a variable resistance in parallel with resistor 714. A second resistor divider network that includes resistors 720 and 722 provides a voltage level for the gate of FET 718. As noted, preferably, a feedback signal, labeled LOAD_AGC, input to FET 718 is preferably proportional to the LINE_AGC feedback signal level developed on the load side.

The AGC amplifier 710 also includes op amp 724 having a fixed gain provided by resistors 726 and 728. The plus input of the op amp 724 is connected to ground via resistor 730, and the minus input of the op amp 724 is connected to resistors 726 and 728 as shown.

The output of the op amp 724 is input to frequency selective circuitry, such as filter 732. Similar to the line processing circuitry the filter 732 is preferably a 2nd order Butterworth high pass active filter, which provides better cut off response than passive filters. However, passive type filter designs, such as LC filters, can also be used.

Preferably, the filter 732 includes an op amp 734 connected to an RC network including capacitors 736, 738 and resistors 740, 742, 744 which perform the filtering function. Utilizing capacitors and resistors in conjunction with the op amp 734 provides a steeper roll off in frequency gain below 500 KHz than would be achieved with passive components alone. Preferably, the internal operating characteristics of the op amp 734 provide the upper limit to the high frequencies passed by the filter 732. To permit maximum utilization of the high frequency characteristics of the op amp 734, the gain of the op amp is preferably set at unity. Filter 732 permits the detection of arc faults even if the AC power lines (including the conductive path) are being used for data communications which typically occur at frequencies below 500 KHz.

The output of the filter 732 is input to the rectifier 750, which is preferably a full wave rectifier. Preferably, the rectifier 750 is configured to rectify input voltages in the millivolt range, and provides a DC voltage for the peak detector 762. The rectifier 750 includes an op amp 752 having its plus input connected to ground and its minus input connected to its feedback path. The rectifier portion provides a variable level of gain, depending on whether the input signal from the filter portion is positive or negative. To illustrate, for positive input signals the gain is zero, and for negative signals, the gain is determined by the ratio of resistors 754 and 756. If the input signal is positive relative to ground, the output of the op amp 752 is negative which pulls the minus input of the op amp down through diode 760 until it is equal to the plus input. Thus, the amplifier has a gain of zero. If, on the other hand, the signal input to the minus input is negative relative to ground, the output of the op amp 752 is positive and feedback current flows through diode 758 and resistor 756 and the gain is set by resistors 754 and 756.

The signal output from the rectifier 750 is in the form of a pulsed DC voltage, which is fed to the peak detector 762. The peak detector 762 has a constant current source that includes op amp 764, diode 766 and resistors 768, 770 and 772. The constant current source is responsive to the pulsed DC voltage from the rectifier 750, the output of which provides a linear charging curve across capacitor 774. Similar to the line processing circuitry 414a, the rate of charging of capacitor 774 is proportional to the number of positive signals input to the peak detector portion from the rectifier 750.

As seen in Fig. 29, capacitor 774 is continually being discharged through resistor 776. In addition, the peak detector 762 functions as an integrator and a time delay circuit which aids in preventing the circuit from reacting to acceptable short lived arcing spikes created when, for example, a switch is thrown or an appliance is plugged in.

The arcing signals being detected by the processing circuitry 414b can be categorized into three main types: high, low and very low arcing signals. In the presence of a high arcing signal, the output of the rectifier 750 includes a substantial number of DC pulses so that the current output by the constant current source rapidly charges the capacitor 774 causing the voltage across the capacitor to reach a zener diode breakdown voltage of output transistor 778 relatively quickly.

When the signal detected is a low arcing signal, the peak detector 762 generates pulses that are more dispersed, causing the voltage across capacitor 774 to rise more slowly, thus delaying the breakover of the zener diode breakdown voltage of transistor 778. In this instance, although resistor 776 continuously discharges the capacitor 774, if the pulses from the rectifier 750 continue for a sufficient enough time to completely charge the capacitor 774, breakover of the zener diode breakdown voltage of transistor 778 can occur.

When the signal detected is a very low arcing signal, the discharge rate of the capacitor 774 via resistor 776 is greater than or equal to the charging rate of the capacitor 774. Thus, the voltage across the capacitor 774 does not reach a sufficiently high level to cause breakover of the zener diode breakdown voltage of transistor 778.

The output of transistor 778, labeled LOAD_OUT, is input to the arc fault trigger generator 700, which as described above, will trigger the SCR 562 causing the solenoid 258 to be energized and contacts 226 and 228 to open or permits resetting of the circuit breaker.

As noted, the output voltage of peak detector 762, designated LINE_AGC, is used as the feedback signal for the AGC amplifier 620 in the line processing circuitry 414a.

Referring to Fig. 30, the arc fault trigger generator 700 of the present application will now be described. Once the output signals from the line processing circuitry (LINE_OUT) and the load processing circuitry (LOAD_OUT) exceed their relative zener diode breakdown voltages, they are fed simultaneously into comparators 780 and 782. The two comparator circuits are similar in construction and like components will be designated with the same reference numerals.

Resistors 784 and 786 provide input resistance to the respective comparator 780 or 782, while resistor 788 provides feedback and resistors 790 and 792 provide adjustable hysteresis for each respective comparator. The output of each comparator 780 and 782 is rectified by a diode 794. In one configuration shown in Fig. 30, the rectified output of each comparator can be converted to a logic "1" or "0" by resistors 798 and 800 and zener diodes 802 and 804 and input to an OR function 796. The output of the OR function 796 would be the arc fault trigger signal, labeled TRIG_AFCI, input to the SCR trigger circuit 564. In addition, the rectified output of comparator 780 can be used to provide, for

example, a visual or audible indication via latch 806 and indicator 808 that a sensed arc fault occurred on the line side.

In another configuration, the rectified output of comparator 780 can be used to provide, for example, a visual or audible indication via indicator 808 that a sensed arc fault occurred on the line side. While, the rectified output of comparator 782 can be used as the arc fault trigger signal to trip or reset the circuit breaker. In this alternative configuration, arc faults sensed on the line side would neither trip the circuit breaker nor permit resetting of the circuit breaker, but arc faults sensed on the load side would.

It should be noted that the LINE_OUT and LOAD_OUT signals are input to both comparators 780 and 782. The LINE_OUT signal is input to the plus input of comparator 780 and the minus input of comparator 782. The LOAD_OUT signal is input to the plus input of comparator 782 and the minus input of comparator 780. In this exemplary configuration, the comparators are prebiased to initially set the outputs of the comparators 780 and 782 low. Thus, if the LINE_OUT signal is greater than the LOAD_OUT signal, the output of comparator 780 goes high, assuming the LINE_OUT signal is greater than the breakover voltage of transistor 694, seen in Fig. 28. If the LOAD_OUT signal is greater than the LINE_OUT signal, the output of comparator 782 goes high, assuming the LOAD_OUT signal is greater than the breakover voltage of transistor 778, seen in Fig. 29.

Therefore, if arcing occurs on the load side of the AFCI/GFCI, the signal generated at the load side pickup will be greater than the signal generated at the line side pickup due to the attenuation of high frequencies caused by the separating impedance. On the other hand, arcing occurring on the line side will generate a larger signal at the line side pickup than at the load side pickup.

In the embodiments described above, both the AFCI and GFCI fault protection capabilities operate to interrupt the AC power by opening contacts 226 and 228 via the actuation of solenoid 258. The solenoid 258 is actuated by triggering the SCR 562 via the SCR trigger circuit 564. As described above, in one embodiment, the SCR trigger circuit 564 can function to provide an OR function to trigger the SCR 562 using known thyristor triggering techniques when either of its two input trigger signals TRIG_GFCI and TRIG_AFCI go active.

When resetting the circuit breaker, the reset operation can be configured so that reset of the circuit breaker can be achieved when one of the two trigger signals, TRIG_GFCI or TRIG_AFCI, go active. In this instance, the SCR trigger circuit 564 would continue to provide the OR function.

However, if the SCR trigger circuit 564 is configured as an OR function, then one of the fault protection operations of the circuit breaker need be operational in order to reset the circuit breaker. To verify that each fault protection operation of the circuit breaker is operational when the circuit breaker is reset, a test operation for each type of fault protection should be provided.

Fig. 31 provides a schematic diagram for an SCR triggering circuit 564 that requires each triggering signal to activate before the SCR 562 is triggered and solenoid 258 is energized when resetting the circuit breaker. In this embodiment, the triggering signals, TRIG_GFCI and TRIG_AFCI, are input to AND gates 820, 822 and 824, as shown, and the output of each AND function is input to an OR gate 826. In addition, a reset enable signal, labeled RESET_ENA, generated by an additional switch in the reset enable switch assembly 270, is also input to the AND gates 820 and 822, as shown. The output of the OR gate 826 is used as the trigger signal for the gate of the SCR 562. In this exemplary configuration, when the circuit breaker is in the 'on' state and the fault protection is armed, the detection of either a ground fault or an arc fault will trigger the SCR 562 via AND gate 822 or 824 and OR gate 826. However, when resetting the circuit breaker, the RESET_ENA signal disables AND gates 822 and 824, and enables AND gates 820. Thus, only the detection of both a ground fault and an arc fault will trigger the SCR 562 via AND gate 820 and OR gate 826 when resetting the circuit breaker.

Similar to the reset operation for the above described embodiments, the circuit breaker is reset by moving the actuator 220 in the direction of arrow F (seen in Fig. 16) to activate reset enable switch assembly 270 (seen in Fig. 31) by closing switches 271a, 271b and 271c, which are preferably momentary switches. Closing switch 271a clocks latch 830 which enables AND gate 820 and disables AND gates 822 and 824. Closing switch 271b triggers pulse generator 273 which outputs a pulse that turns on oscillator 275 for a finite period of time at a resonant frequency of about 1.5 MHz. An example of a suitable pulse

is a 10 ms pulse at low current, in the order of about 1-10 mA. It should be noted that the number of turns on the coil 592 on the transformer assembly 552 can be used to control the current from the transformer assembly. If the arc fault circuit interrupting portion is operational, activation of switch 271b simulates an arc fault so that the arc fault trigger signal, TRIG_AFCI, is active. Closing switch 271c simulates a ground fault so that the ground fault trigger signal, TRIG_GFCI, is active. When TRIG_GFCI goes active, SCR 832 turns on thereby turning on transistor 834 so that a logic 1 is seen by AND gate 820.

In this configuration, when the latch 830 is clocked and the TRIG_AFCI and TRIG_GFCI lines are active, AND gate 820 outputs a logic 1 which triggers the SCR 562 to energize solenoid 258.

The output of AND gate 820 is also connected to the reset input of the latch 830 via inverter 836. As a result, when AND gate 820 outputs a logic 1, latch 830 is reset, so that gate 820 is disabled and gates 822 and 824 are enabled for standard operation of the breaker. It may be desirable to include a delay line 838 (shown in phantom in Fig. 31), which provides a time delay that is sufficient to allow the mechanical components of the circuit breaker to reset before enabling AND gates 822 and 824 to avoid false triggering of the circuit breaker.

Systems Having Circuit Breakers With Reset Lockout

The circuit breakers described above can be used in electrical distribution systems in, for example, a home, shown in the exemplary block diagram of Fig. 32. The system includes a circuit breaker panel 300 used to supply electrical power to various circuits in the home, at least one GFCI circuit breaker having a reset lockout and/or independent trip portions installed in the panel, and various connection points, such as receptacles, to connect one or more loads thereto. As is well known, the line phase connection 212 of the GFCI circuit breaker is connected to a power distribution bus 302 in the panel and the load phase connection 214 is connected to the phase conductor 304 feeding one or more loads. A neutral conductor 306 to the one or more loads is connected to a load neutral connection 218 associated with the circuit breaker 200, and a line neutral conductor 216, typically, extending from the circuit breaker housing is connected to a neutral bus 308 in the panel.

while there have been shown and described and pointed out the fundamental features of the invention, it will be understood that various omissions and substitutions and changes of the form and details of the device described and illustrated and in its operation may be made by those skilled in the art, without departing from the spirit of the invention.

Throughout this specification and the claims which follow, unless the context requires otherwise, the word "comprise", and variations such as "comprises" or "comprising", will be understood to imply the inclusion of a stated integer or step or group of integers or steps but not the exclusion of any other integer or step or group of integers or steps.

The reference to any prior art in this specification is not, and should not be taken as, an acknowledgement or any form of suggestion that that prior art forms part of the common general knowledge in Australia.

The claims defining the invention are as follows:

1. A circuit breaker including:

housing means;

line and load connection means accessible from an exterior of said housing means for connecting to external wiring;

means for conducting electricity between said line and load connection means, said means for conducting electricity including switch means for opening and closing said means for conducting electricity;

circuit interrupting means disposed within said housing means for causing said switch means to open in response to the occurrence of a predefined condition;

reset lockout means responsive to activation of said circuit interrupting means for inhibiting closing of said switch means after said circuit interrupting means causes said switch means to open; and

reset means for activating said circuit interrupting means so that said reset lockout means does not inhibit closing of said switch means, and for closing said switch means.

2. The circuit breaker according to claim 1, wherein said predefined condition includes a fault or an over-current condition.

3. The circuit breaker according to claim 2, wherein said fault includes a ground fault, an arc fault, an immersion detection fault, an appliance leakage fault or an equipment leakage fault.

4. The circuit breaker according to claim 1 further including trip means for causing said switch means to open independently of the operation of said circuit interrupting means.

5. The circuit breaker according to claim 4, wherein said circuit interrupting means includes sensing means for sensing ground faults associated with conducted electricity and means for causing said switch means to open said means for conducting electricity.

6. The circuit breaker according to claim 5, wherein said reset means includes:

a manually operated actuator operatively coupled to said reset lockout means; and

reset enable switch means capable of being activated by operation of said actuator for simulating a ground fault in said sensing means so as to activate said circuit interrupting means.

7. The circuit breaker according to claim 6, wherein said reset enable switch means includes a fixed contact that is energized by said operation of said actuator to simulate the ground fault.

8. The circuit breaker according to claim 6, wherein said reset enable switch means includes a pair of momentary switches which when actuated switch power supplied to said sensing means from said load connection means to said line connection means, and simulate the ground fault.

9. The circuit breaker according to claim 6, wherein said reset enable switch means includes a plurality of switch contacts that are sequentially activated to first switch power supplied to said sensing means from said load connection means to said line connection means, and second to simulate the ground fault.

10. A method for testing the operation of a circuit breaker having a housing with line and load phase connections accessible from an exterior surface of said housing, and a conductive path between said line and load phase connections, said method including:

manually activating a trip portion of the circuit breaker to open said conductive path and to enable a reset lockout portion that inhibits closing said conductive path; and

activating a reset portion to perform a reset operation, wherein during said reset operation a circuit interrupting portion is activated, and wherein if the circuit interrupting portion is operational, the circuit interrupting portion disables the reset lockout portion and facilitates closing of said conductive path, and wherein if the circuit interrupting portion is non-operational, the reset lockout portion remains enabled so that closing said conductive path is inhibited.

11. The method according to claim 10 wherein said circuit breaker is a GFCI circuit breaker.

12. The method according to claim 10 wherein said circuit breaker is an AFCI circuit breaker.

13. A power distribution system including:

a source of electricity;

at least one load;

a circuit breaker regulating power from said source of electricity to said at least one load, said circuit breaker includes:

housing means;

line and load connection means accessible from an exterior of said housing means for connecting to external wiring;

means for conducting electricity between said line and load connection means, said means for conducting electricity including switch means for opening and closing said means for conducting electricity;

circuit interrupting means disposed within said housing means for causing said switch means to open in response to the occurrence of a fault;

reset lockout means responsive to activation of said circuit interrupting means for inhibiting closing of said switch means after said circuit interrupting means causes said switch means to open; and

reset means for activating said circuit interrupting means so that said reset lockout means does not inhibit closing of said switch means, and for closing said

switch means.

14. The power distribution system according to claim 13, wherein said circuit breaker further includes trip means for causing said switch means to open independently of the operation of said circuit interrupting means.

15. The power distribution system according to claim 13, wherein said fault is a ground fault.

16. The power distribution system according to claim 13 wherein said fault is an arc fault.

17. A circuit breaker as substantially hereinbefore described with reference to the accompanying drawings.

18. A method for testing the operation of a circuit breaker as substantially hereinbefore described.

19. A power distribution system as substantially hereinbefore described with reference to the accompanying drawings.

FIG. 1

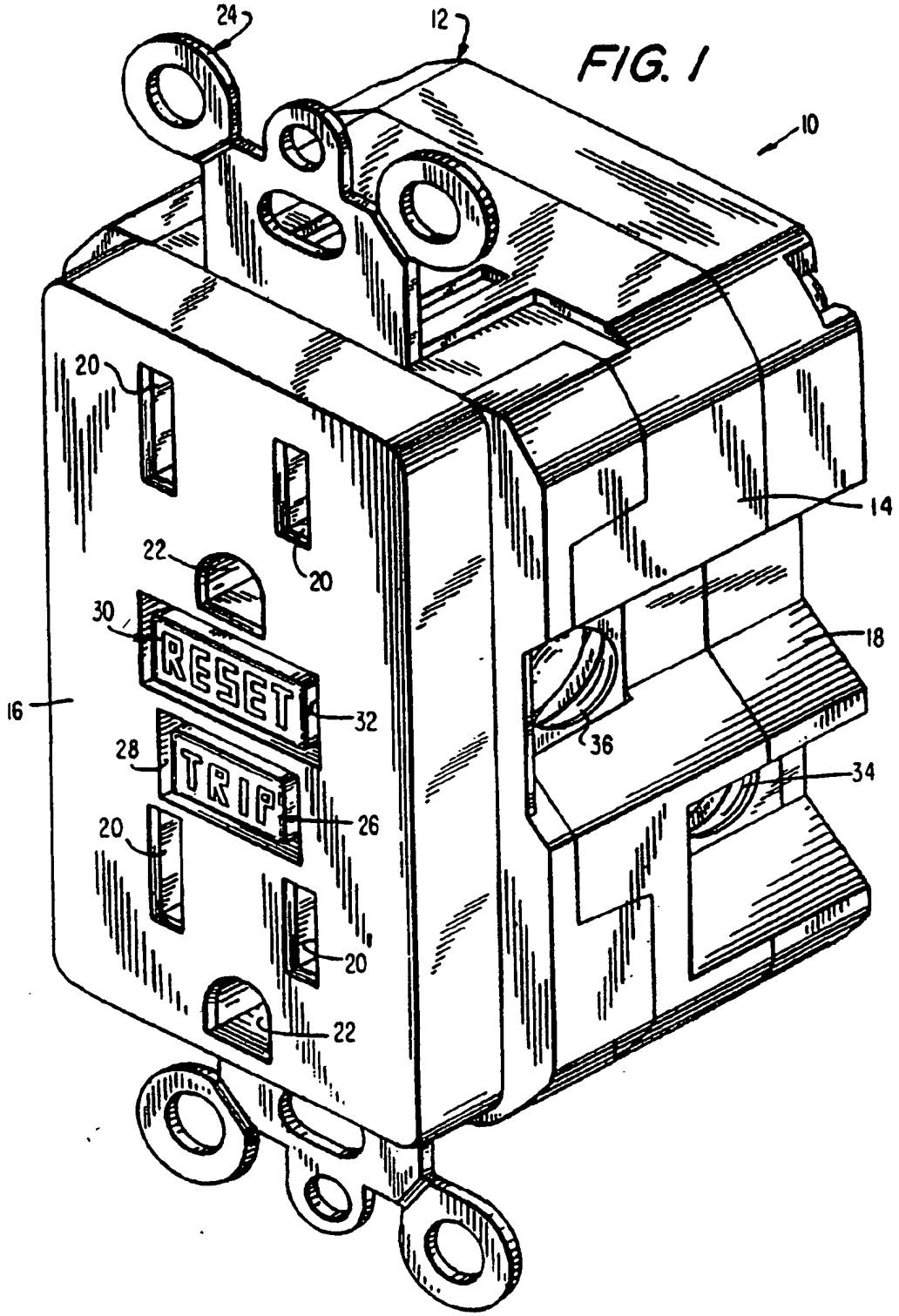
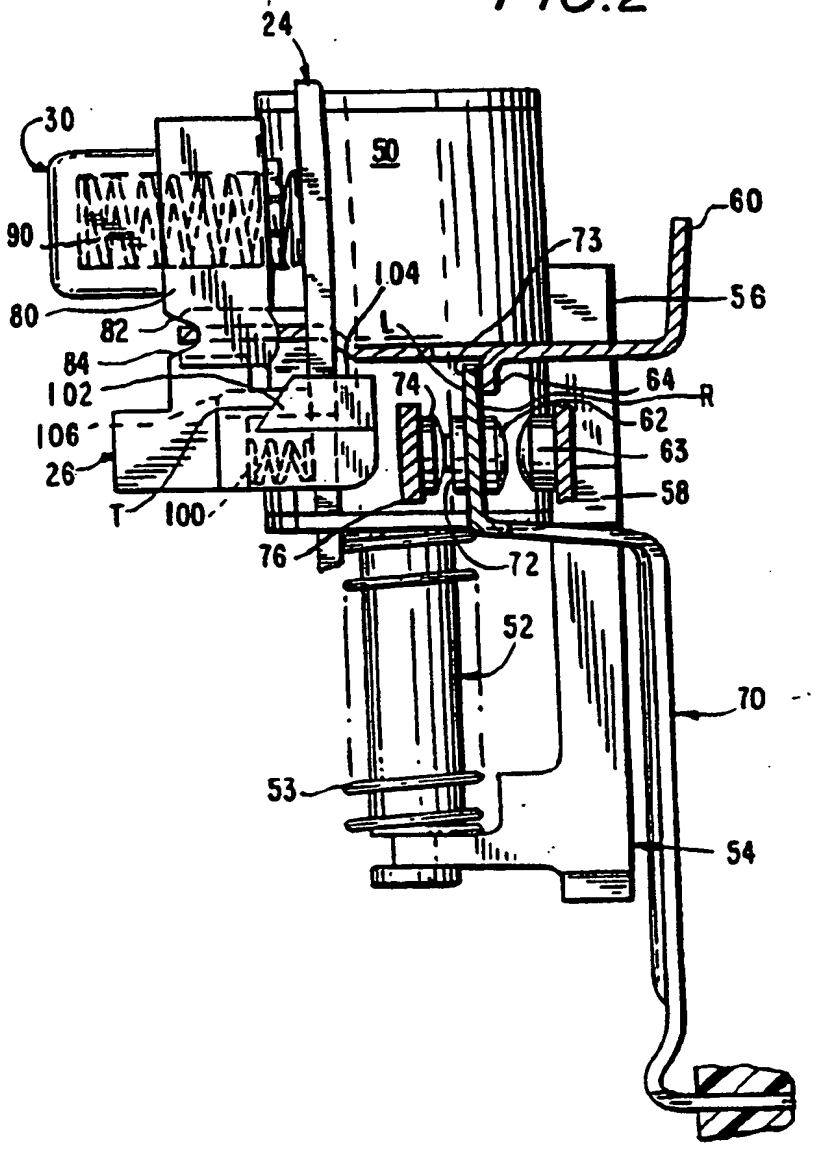


FIG.2


24
30
50
60
90
73
104
56
80
82
L
84
74
64
R
102
62
106
63
26
58
T
100
76
72
52
70
53
54

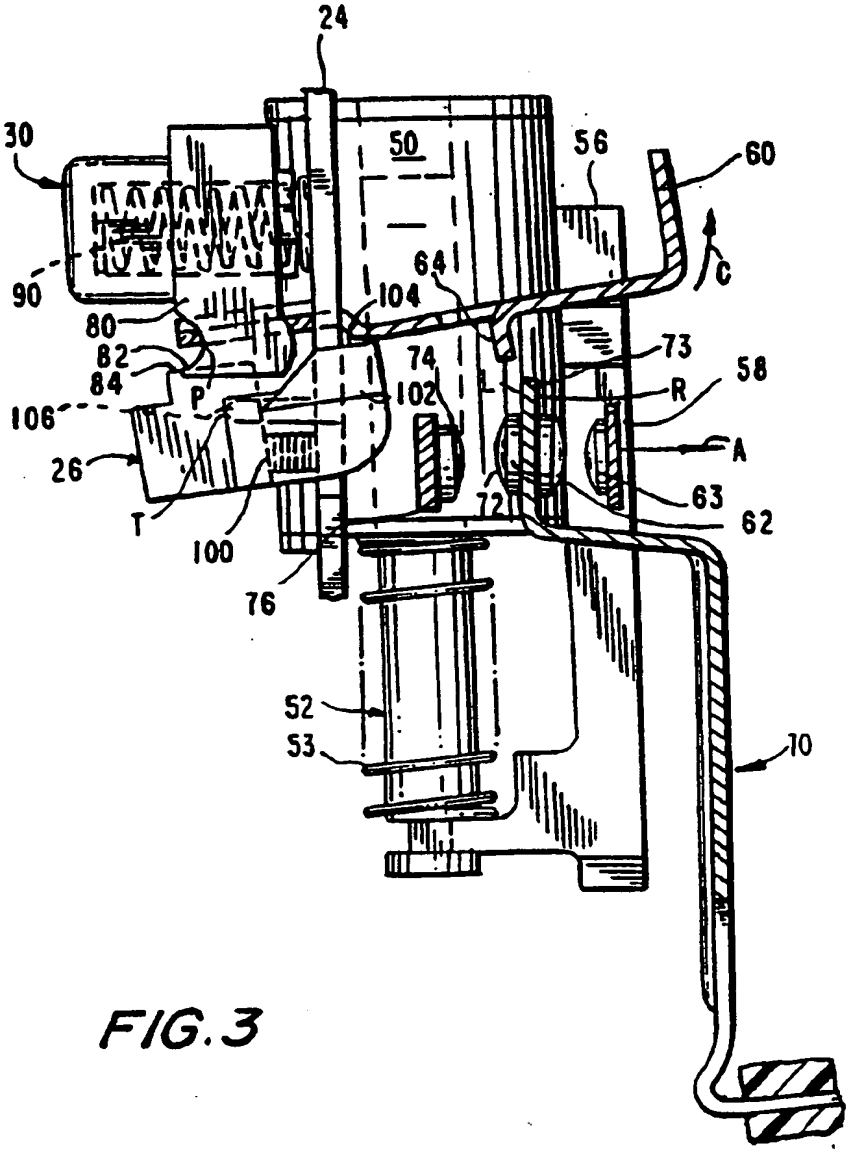

24
30
50
56
60
C
90
64
104
80
73
82
74
58
84
P
102
R
106
A
26
63
72
62
T
100
76
52
53
10

FIG. 3

FIG. 4

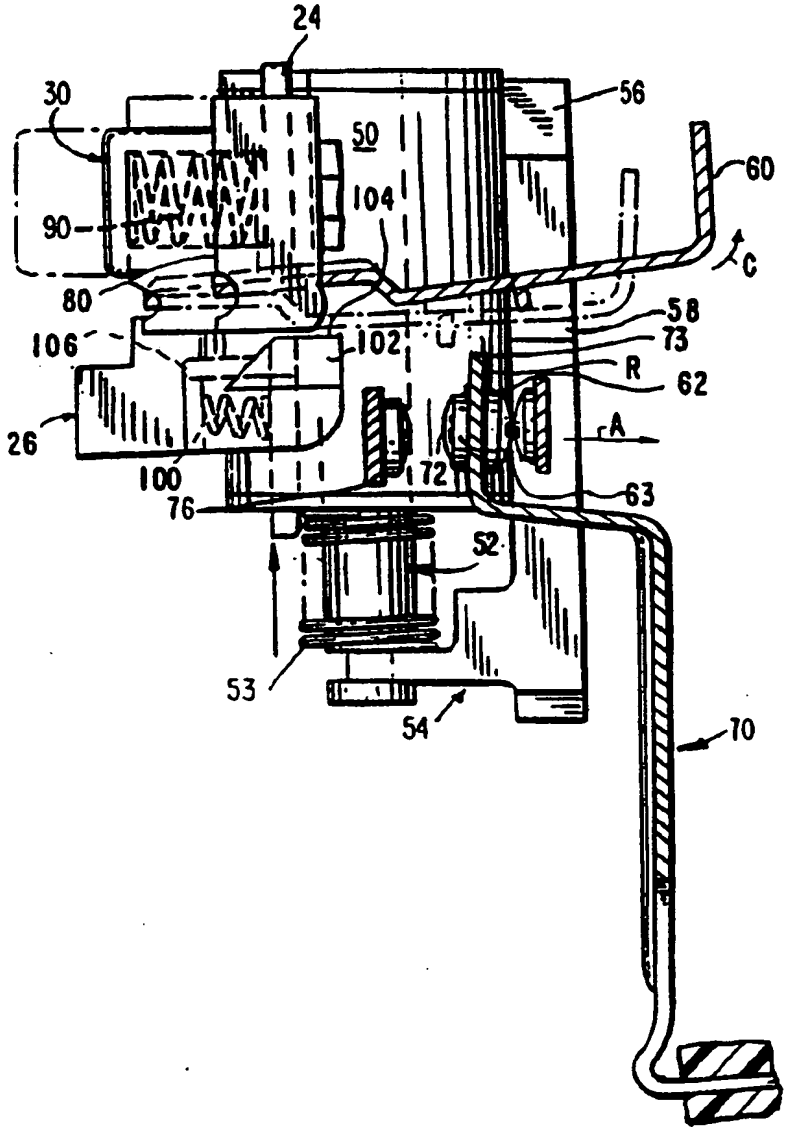

24
30
56
50
60
104
90
C
80
58
106
102
73
R
62
26
A
100
72
63
76
52
53
54
70

FIG. 5

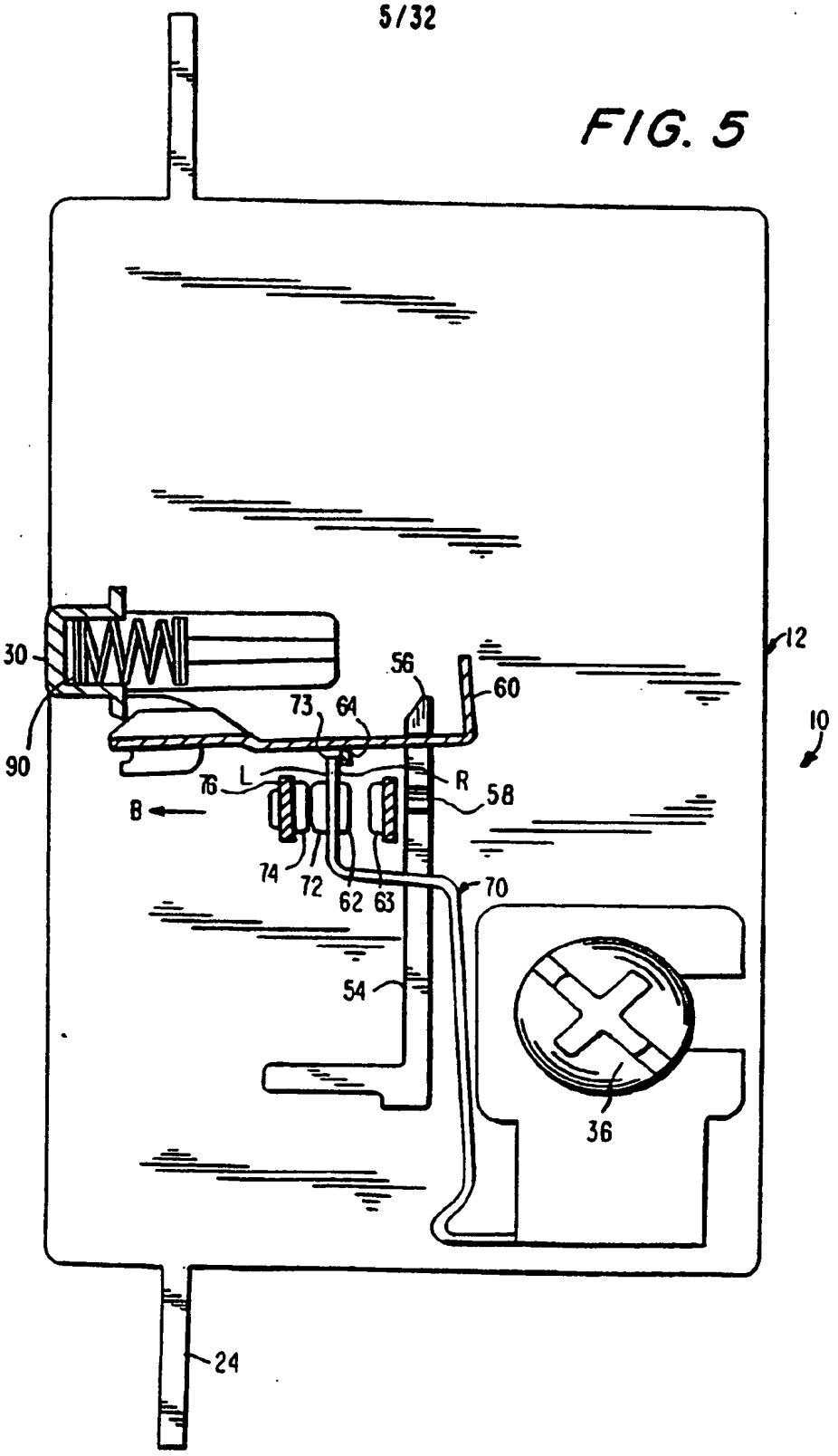


FIG.6

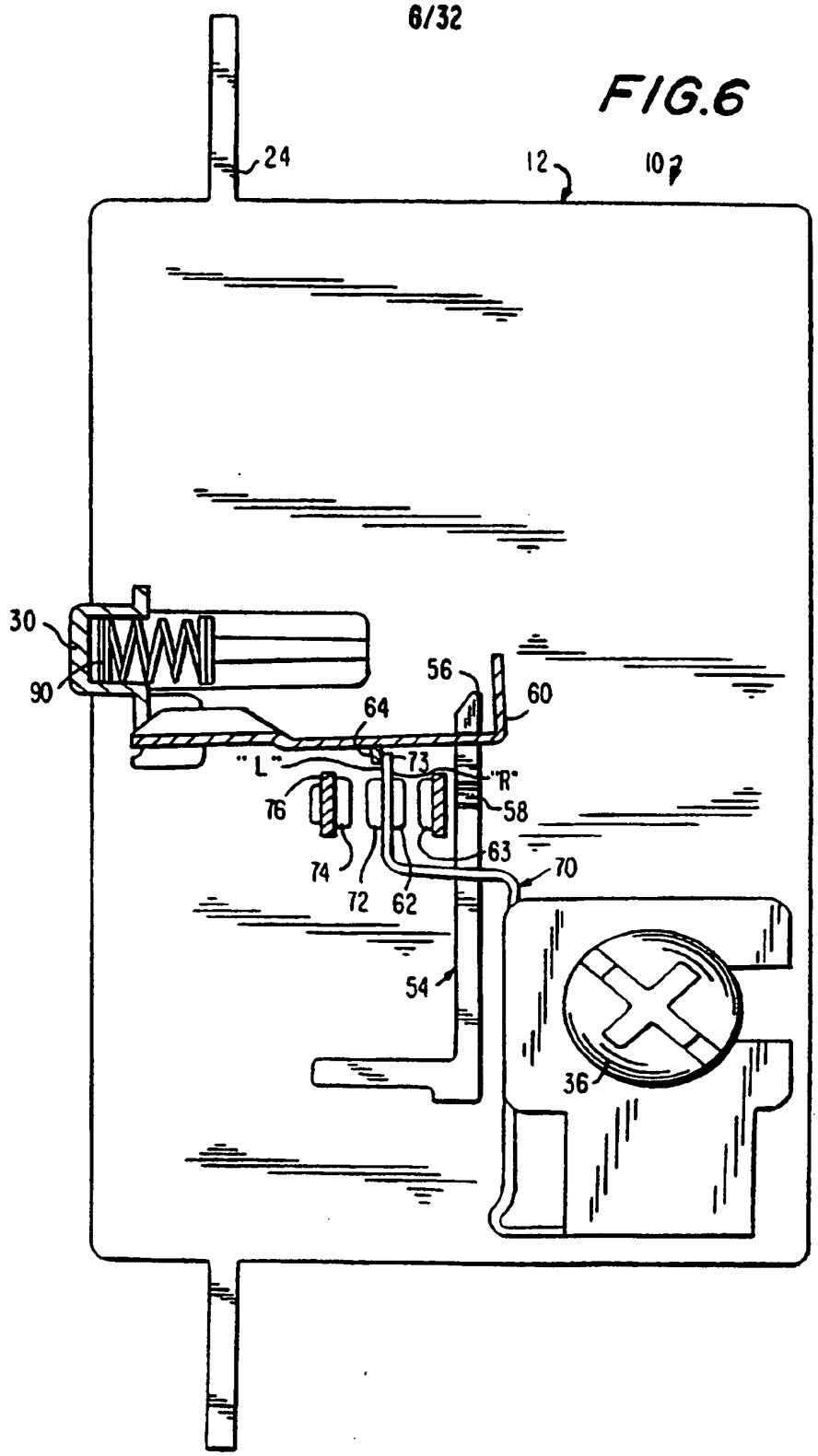
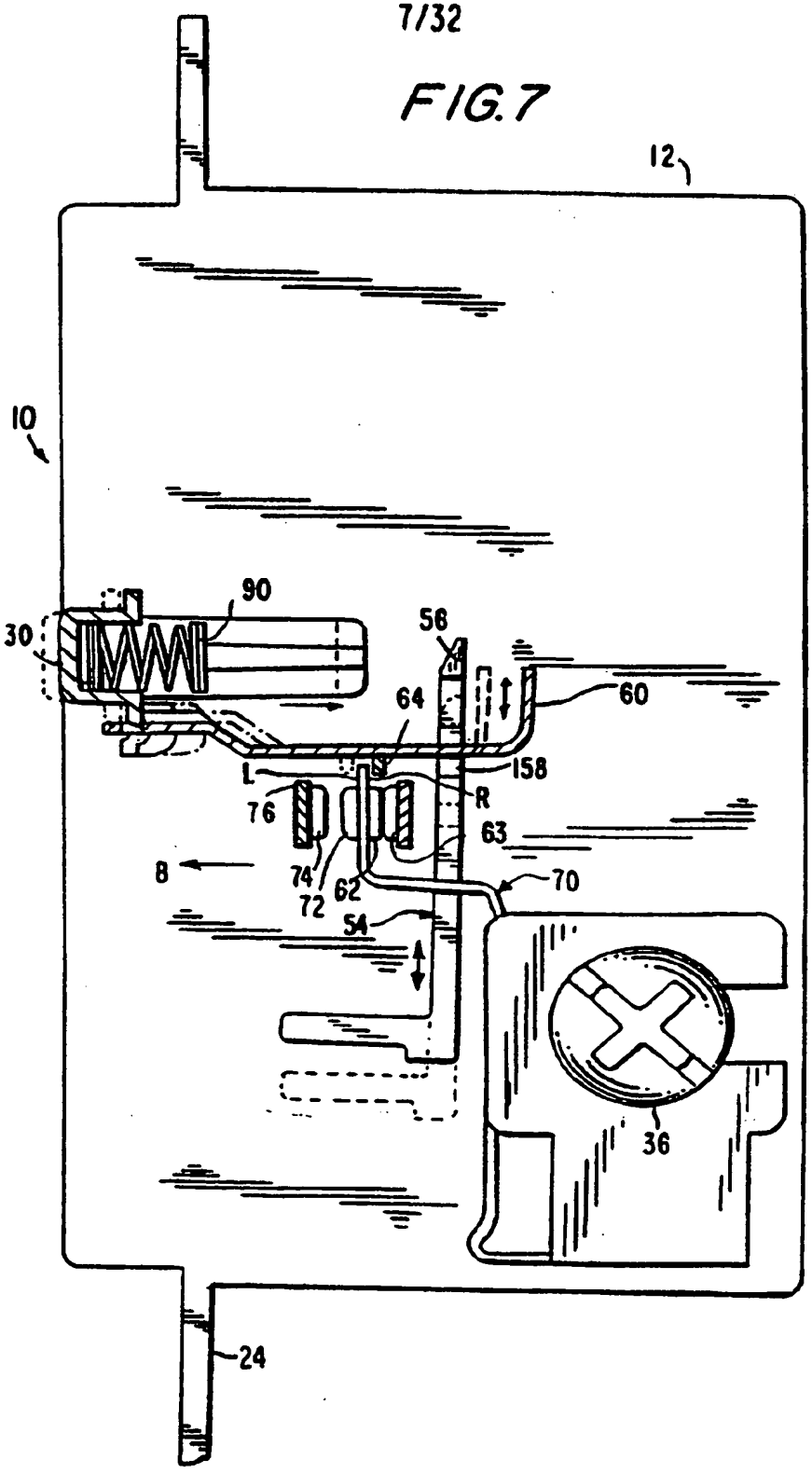


FIG. 7



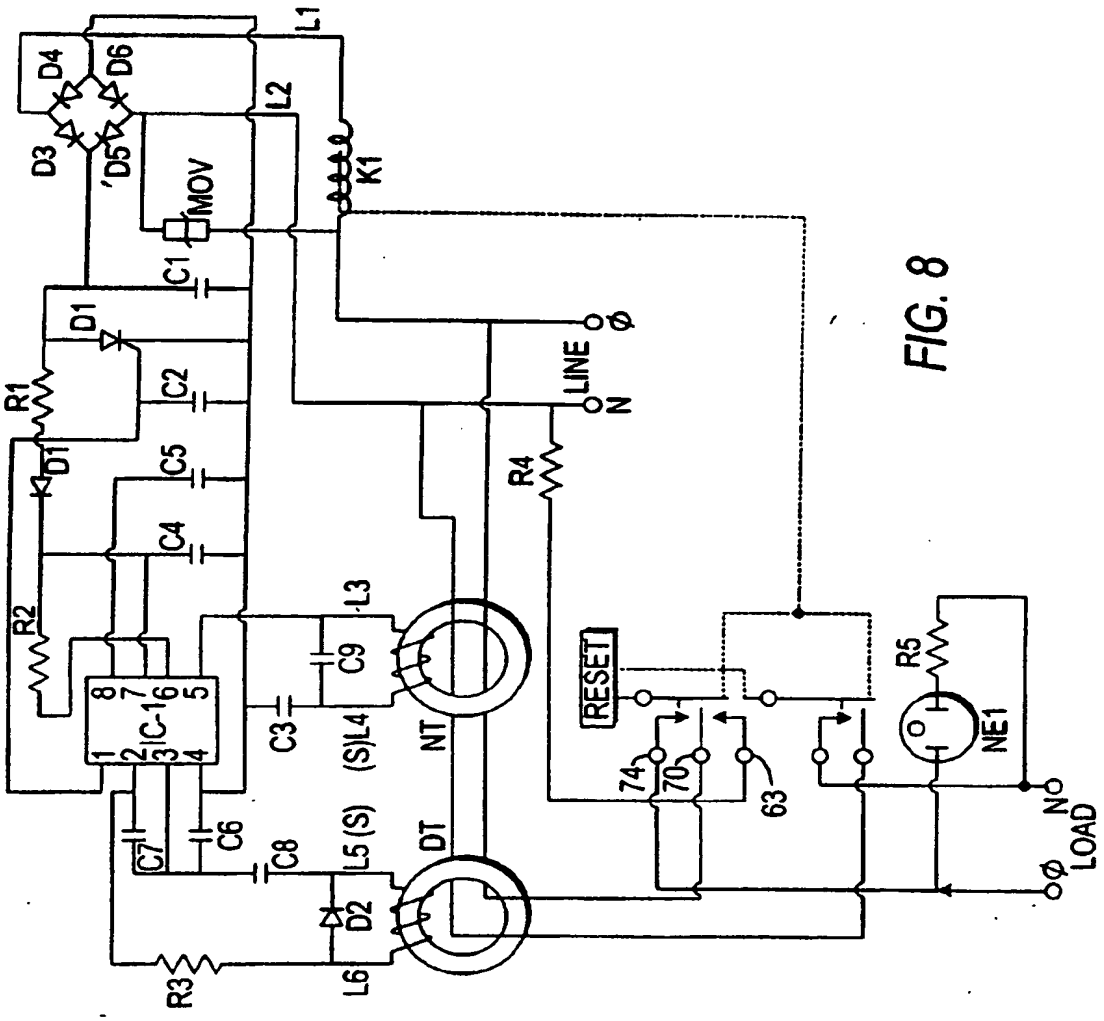
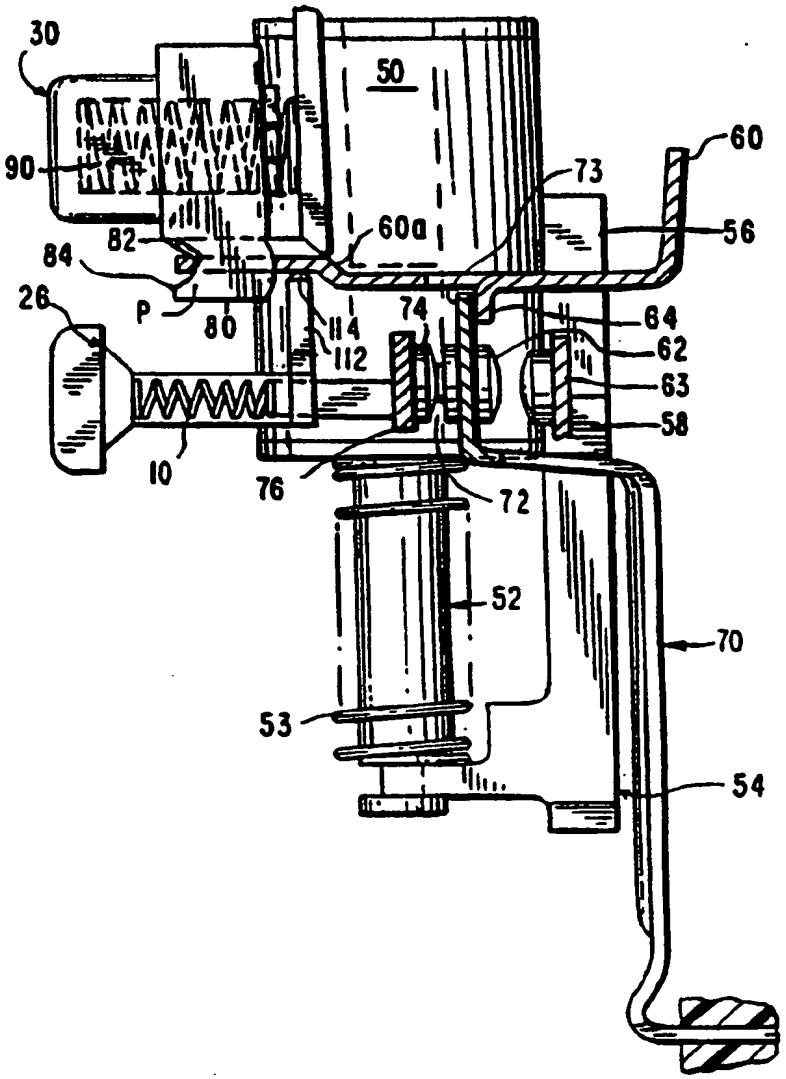

L1
D4
D6
L2
D3
D5
MOV
K1
C1
D1
R1
C2
LINE
Ø
N
D1
C5
R4
C4
L3
R2
C9
RESET
R5
IC-1
C3
(S)L4
NT
NE1
74
70
63
N
C6
C7
C8
L5 (S)
DT
LOAD
Ø
D2
R3
L6

FIG. 8

FIG. 9


30
50
90
60
73
56
82
60a
84
26
P
80
114
112
74
64
62
63
58
10
76
72
52
70
53
54

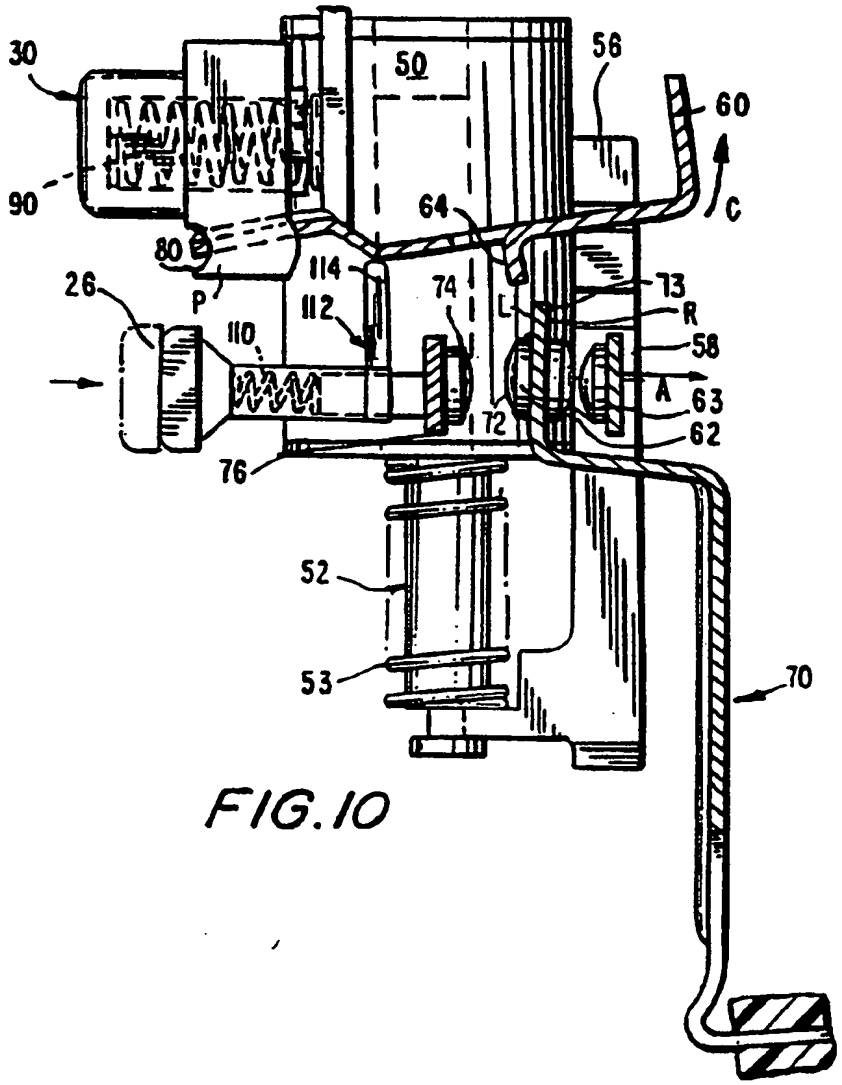

30
50
56
60
C
90
64
80
114
26
P
112
74
L
73
R
58
110
A
63
72
62
76
52
53
70

FIG. 10

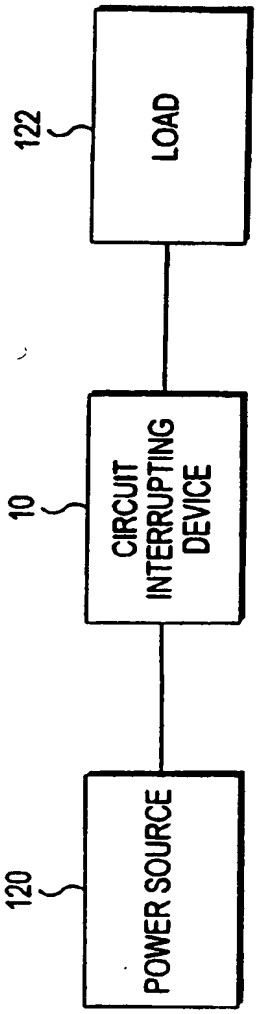


FIG. 11

FIG. 12

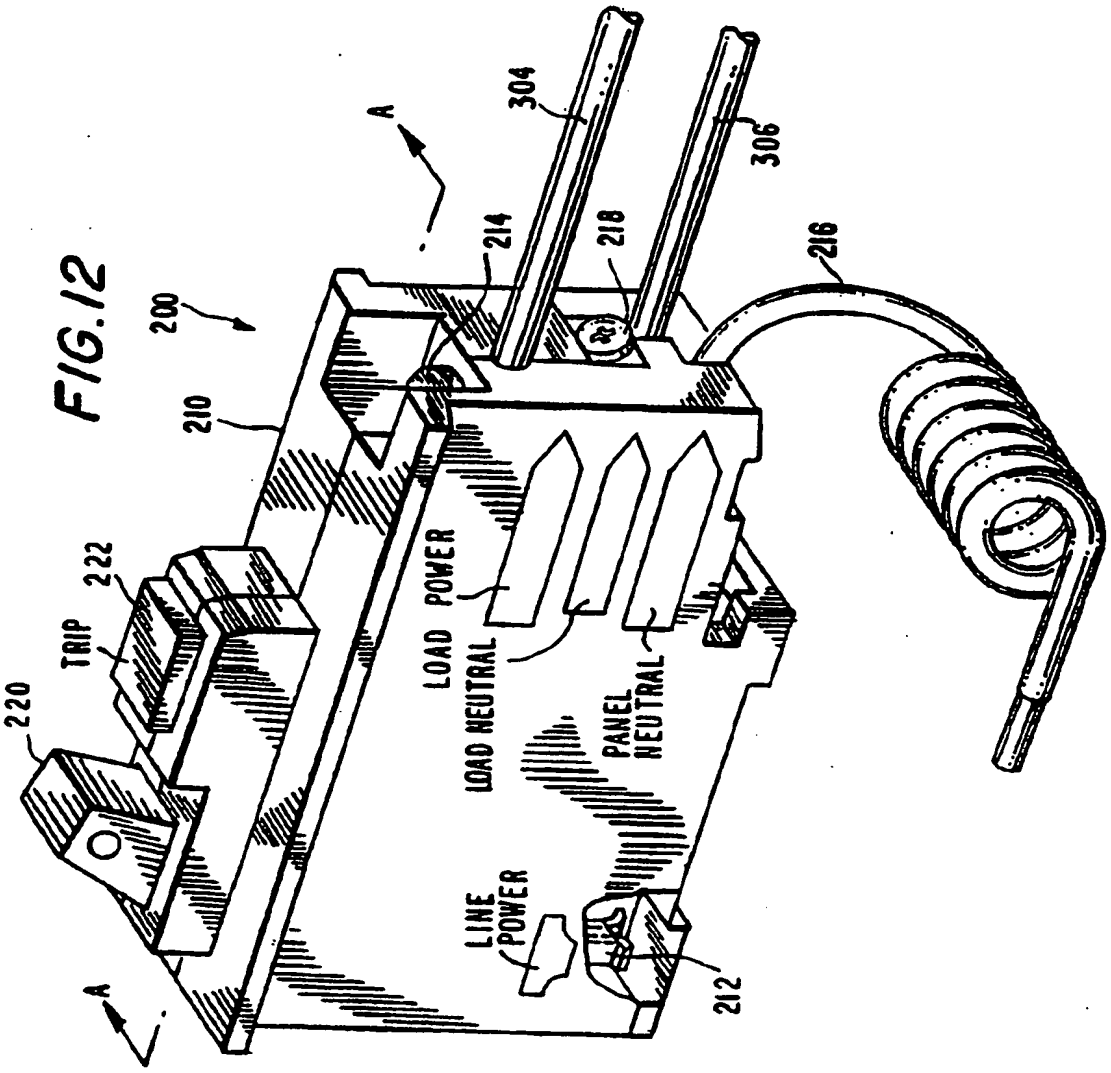

A
304
306
214
218
216
200
210
222
TRIP
220
LOAD POWER
LOAD NEUTRAL
PANEL NEUTRAL
LINE POWER
212
A

FIG. 13

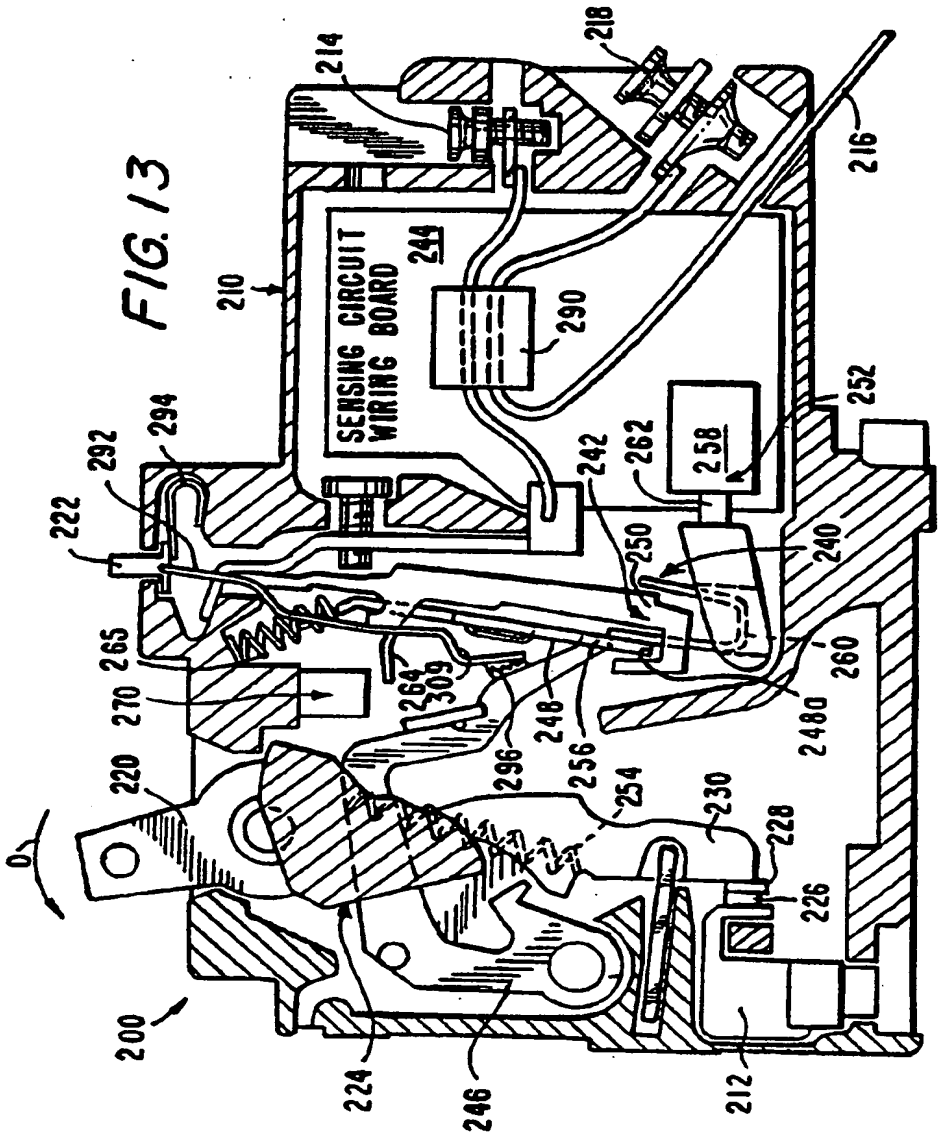

SENSING CIRCUIT WIRING BOARD
244
210
214
218
216
290
292
294
222
242
262
258
252
250
240
265
270
264
309
248
256
296
254
230
228
226
220
260
248a
200
224
246
212

FIG. 14

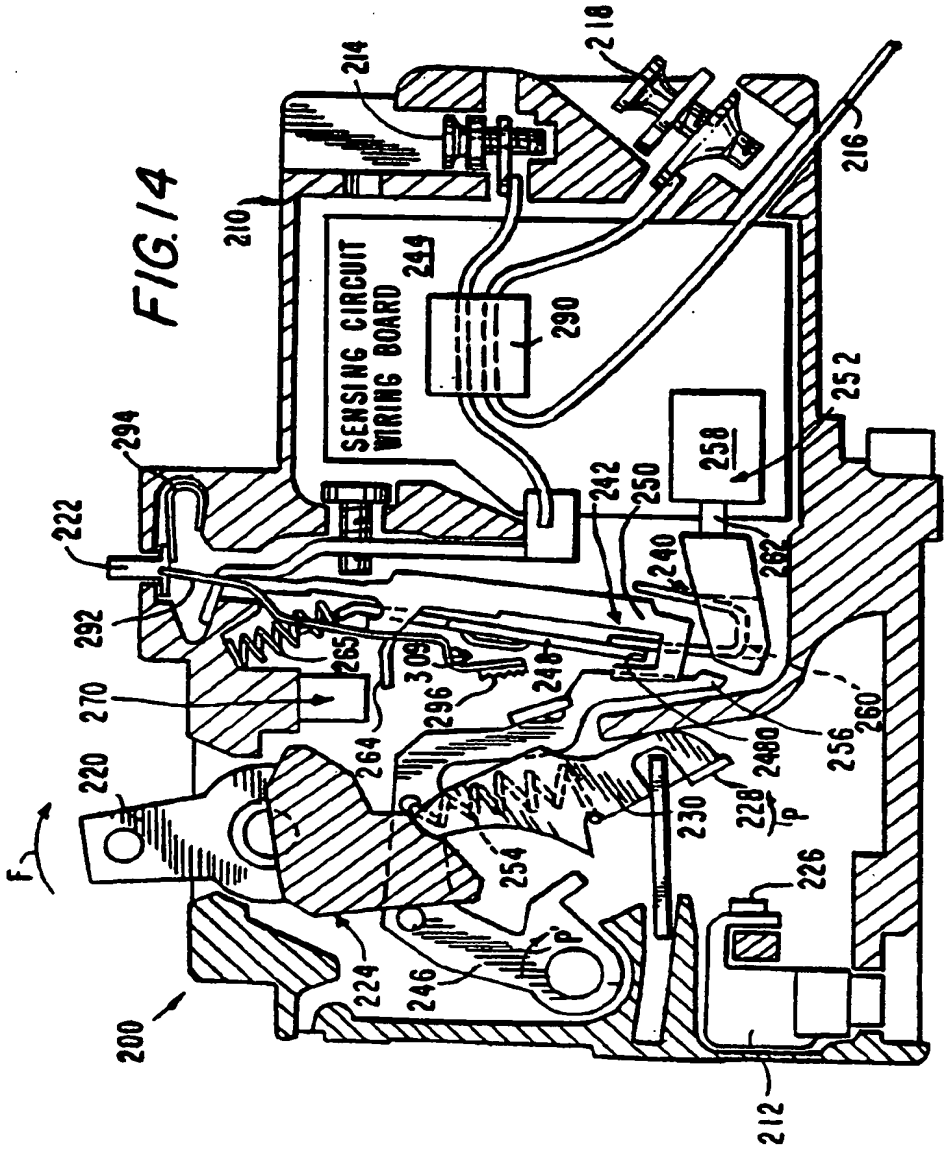

SENSING CIRCUIT WIRING BOARD
244
290
210
214
218
216
252
258
294
222
242
250
240
262
292
265
308
296
246
270
264
260
256
248
220
228
230
254
226
224
246
200
212
F
P
P'

FIG.15

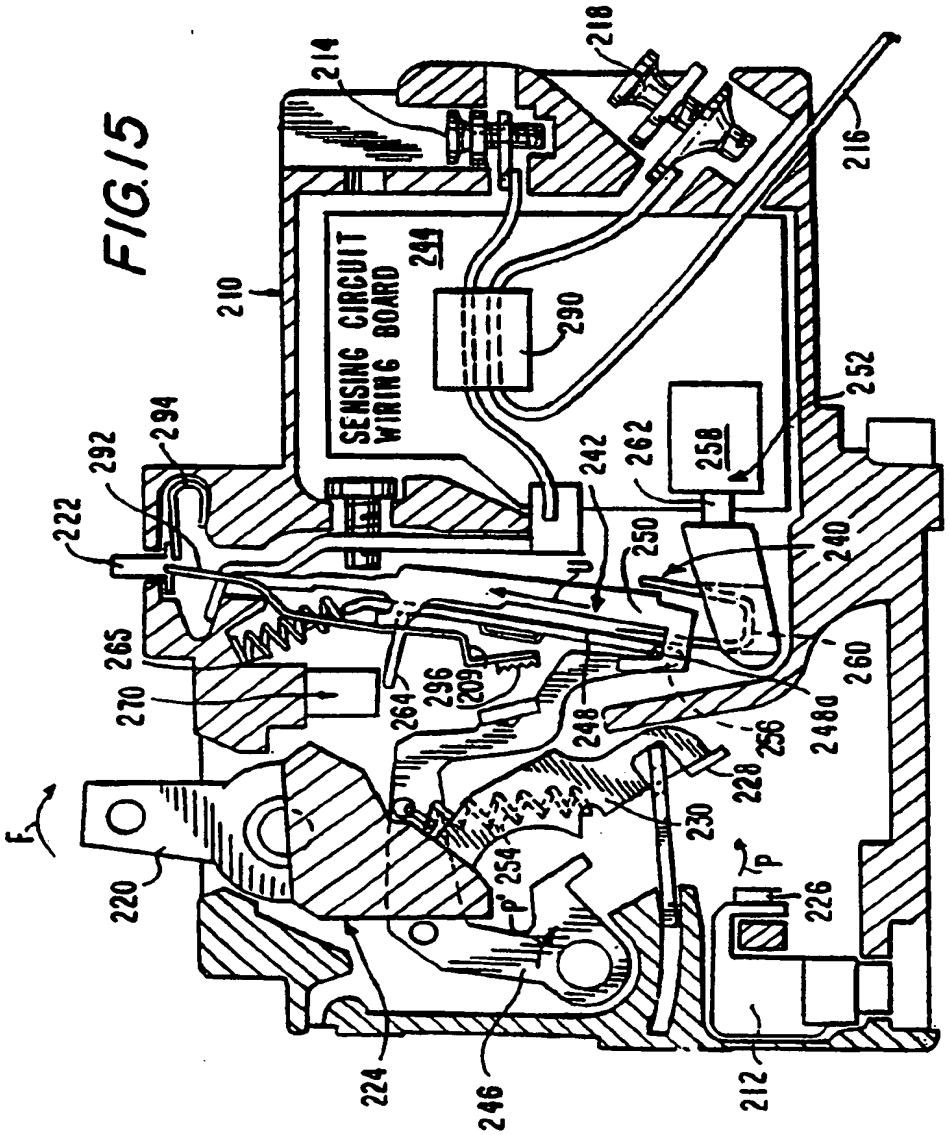

SENSING CIRCUIT WIRING BOARD
244
210
214
218
216
290
252
258
262
242
294
292
222
250
240
265
270
264
296
209
248
260
248a
256
228
230
254
220
226
224
246
212

FIG. 16

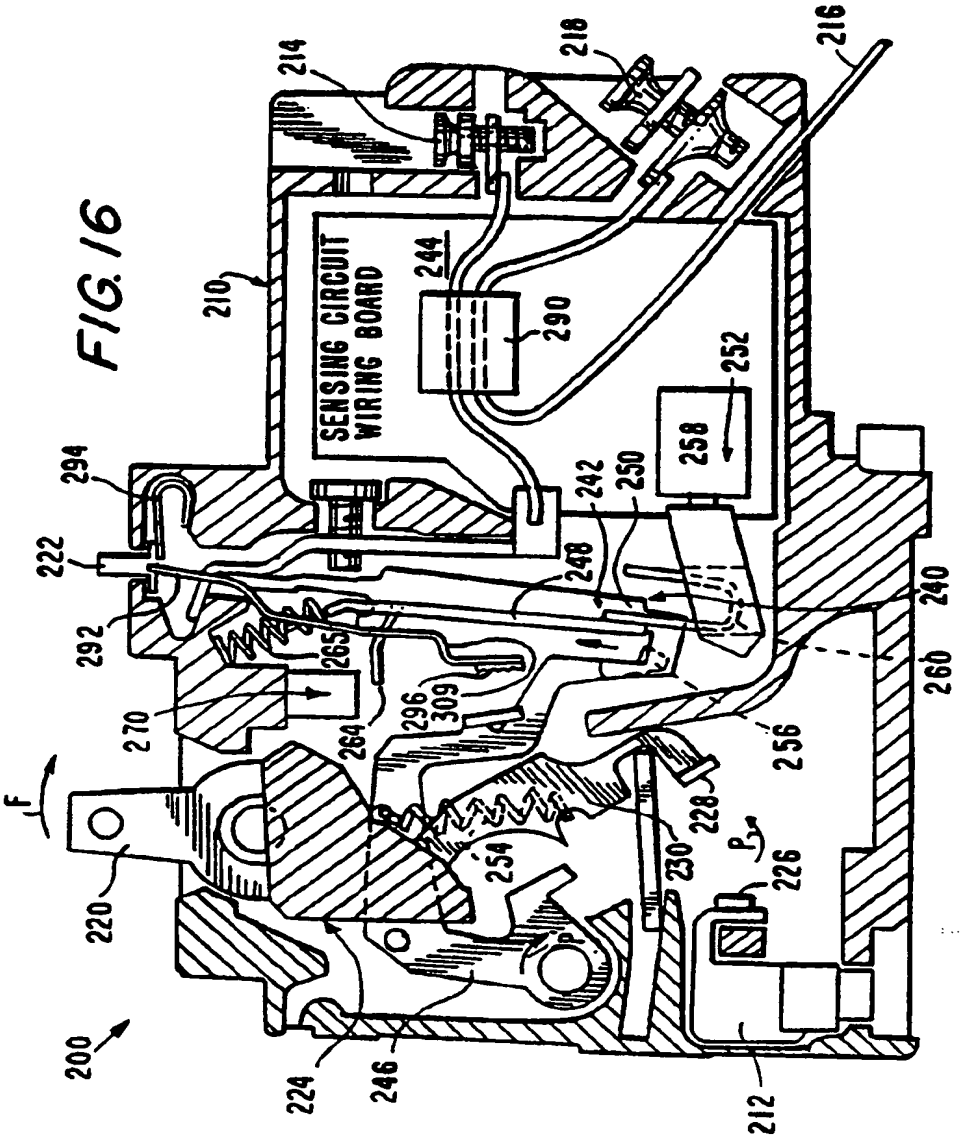

SENSING CIRCUIT WIRING BOARD
200
210
212
214
216
218
220
222
224
226
228
230
240
242
244
246
248
250
252
254
256
258
260
264
265
270
290
292
294
296
309
F

FIG.17

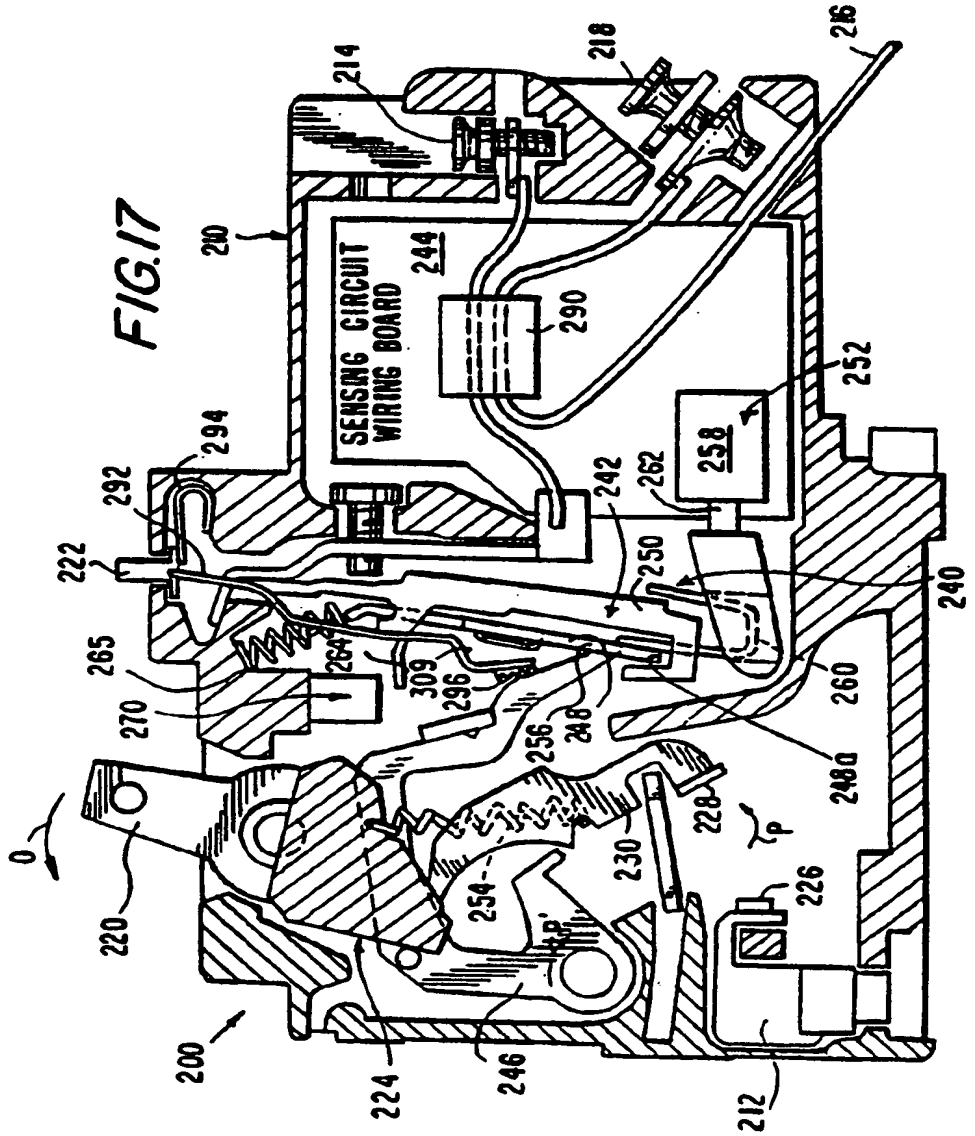
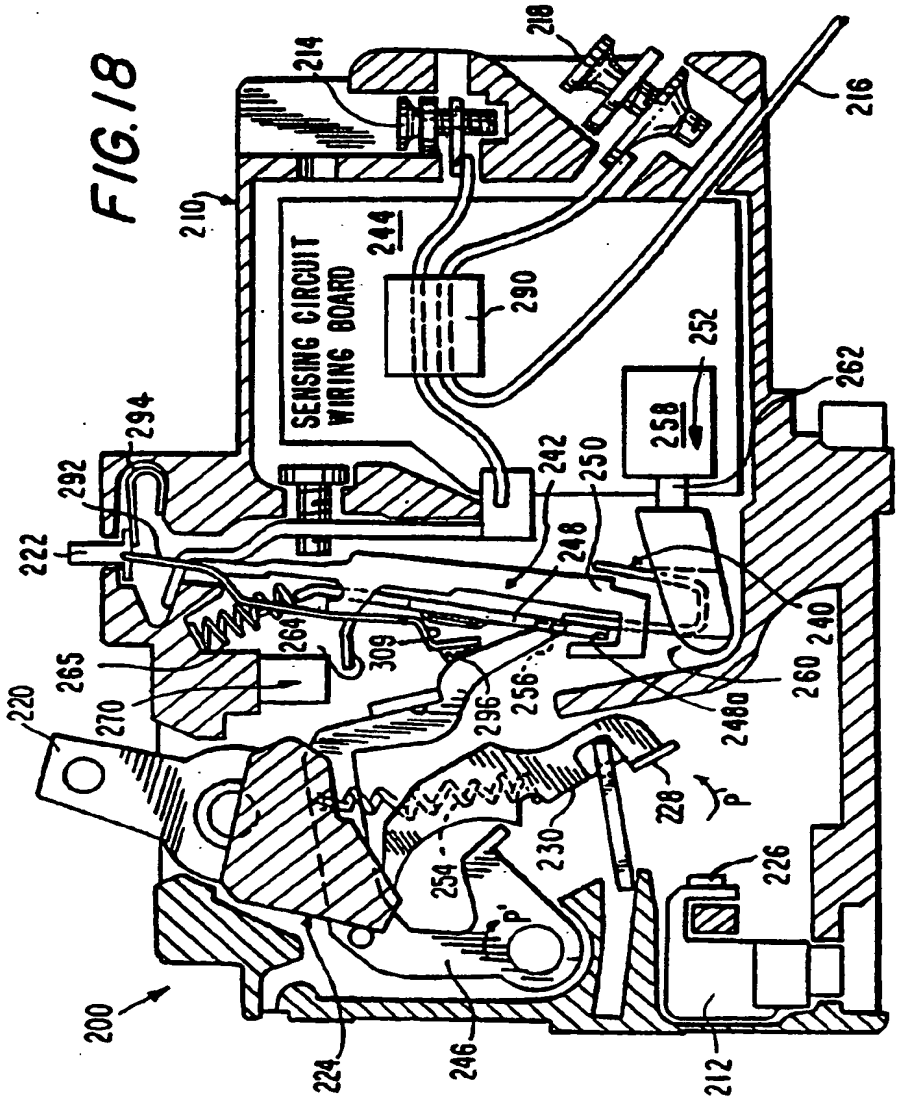

SENSING CIRCUIT WIRING BOARD
244
290
218
214
26
280
252
258
294
292
242
262
222
250
240
265
284
309
296
260
270
256
248
240a
228
230
254
226
220
200
224
246
212

FIG. 18


SENSING CIRCUIT
WIRING BOARD
244
290
252
258
262
294
292
222
242
250
248
240
264
309
265
270
220
296
256
260
248a
228
P
230
254
226
P'
200
224
246
212
210
214
218
216

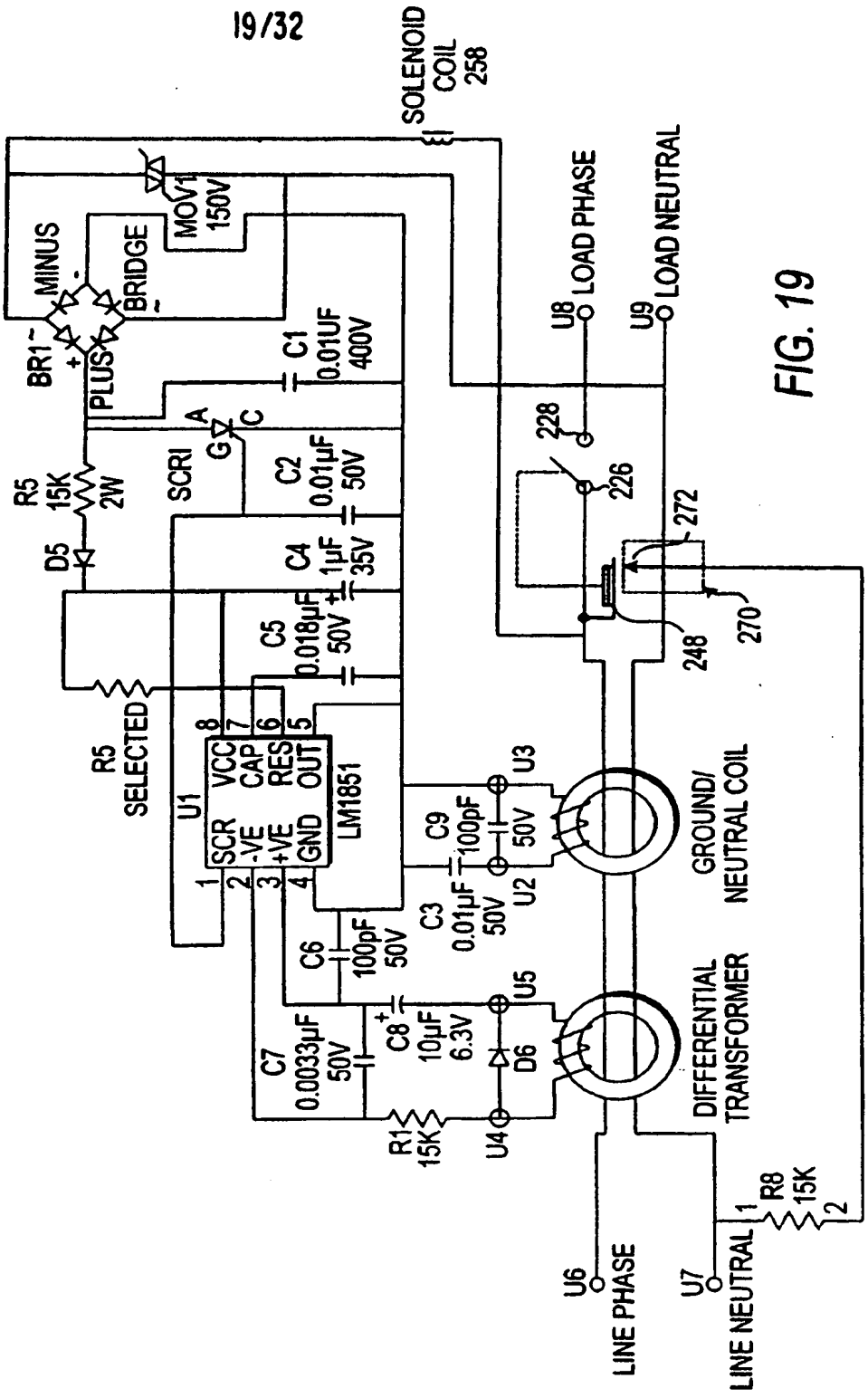

SOLENOID COIL 258
MOV1 150V
MINUS
BRIDGE
BR1
PLUS
C1 0.01UF 400V
U8 LOAD PHASE
U9 LOAD NEUTRAL
228
226
272
270
248
R5 15K 2W
D5
SCR1
A
G
C
C2 0.01µF 50V
C4 1µF 35V
C5 0.018µF 50V
R5 SELECTED
U1
VCC
CAP
RES
OUT
SCR
-VE
+VE
GND
LM1851
C9 100pF 50V
U3
U2
C3 0.01µF 50V
C6 100pF 50V
C7 0.0033µF 50V
C8 10µF 6.3V
U5
D6
R1 15K
U4
GROUND/ NEUTRAL COIL
DIFFERENTIAL TRANSFORMER
R8 15K
U6 LINE PHASE
U7 LINE NEUTRAL

FIG. 19

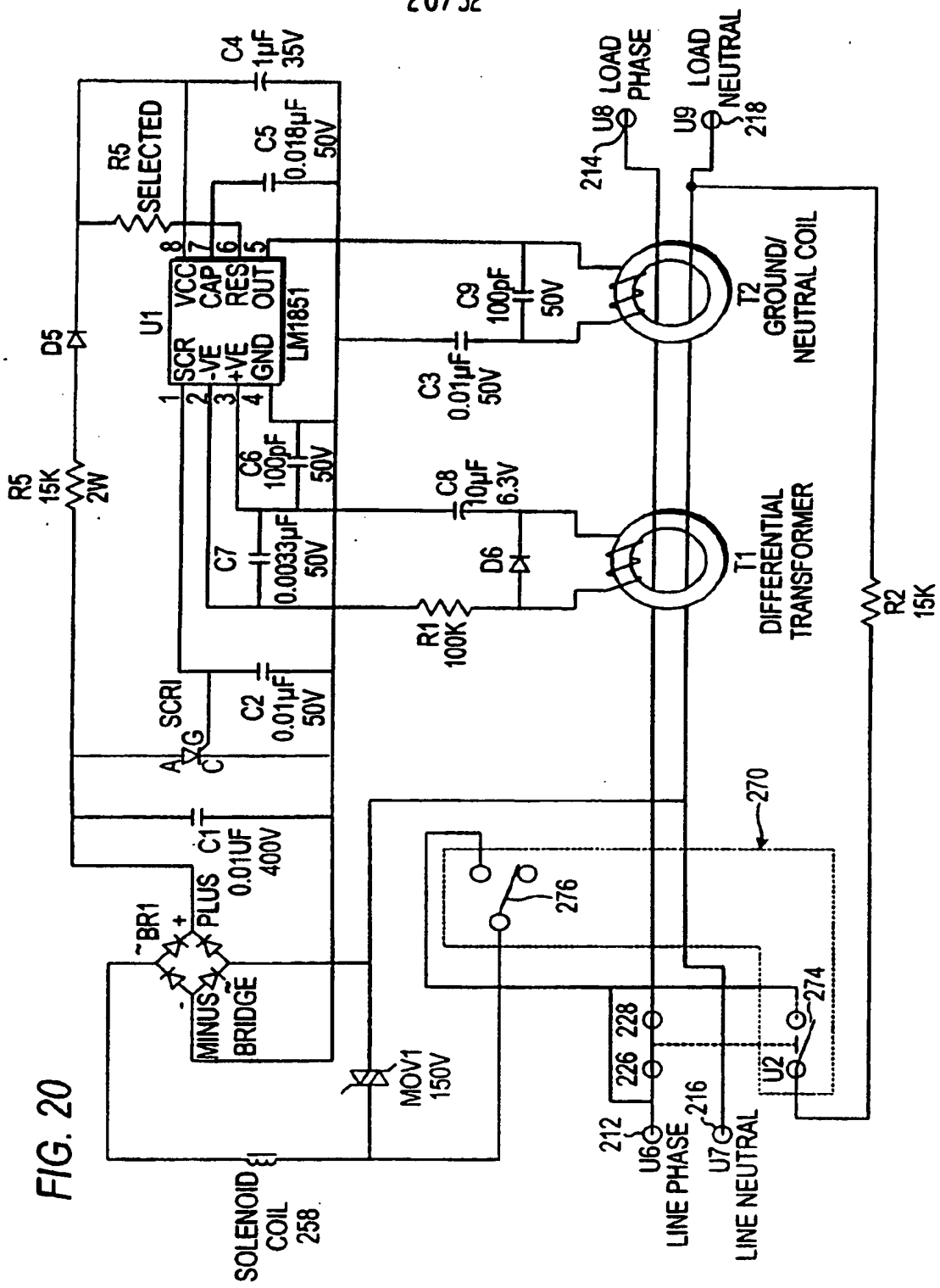

C4 1µF 35V
C5 0.018µF 50V
R5 SELECTED
U1
VCC CAP RES OUT
SCR -VE +VE GND
LM1851
D5
R5 15K 2W
C6 100pF 50V
C7 0.0033µF 50V
C3 0.01µF 50V
C9 100pF 50V
C8 10µF 6.3V
D6
R1 100K
C2 0.01µF 50V
SCRI
A G C
C1 0.01UF 400V
~BR1
PLUS
MINUS
BRIDGE
MOV1 150V
SOLENOID COIL 258
U8 LOAD PHASE
U9 LOAD NEUTRAL
214
218
T2 GROUND/ NEUTRAL COIL
T1 DIFFERENTIAL TRANSFORMER
R2 15K
270
276
274
U2
226 228
212
U6 LINE PHASE
216
U7 LINE NEUTRAL

FIG. 20

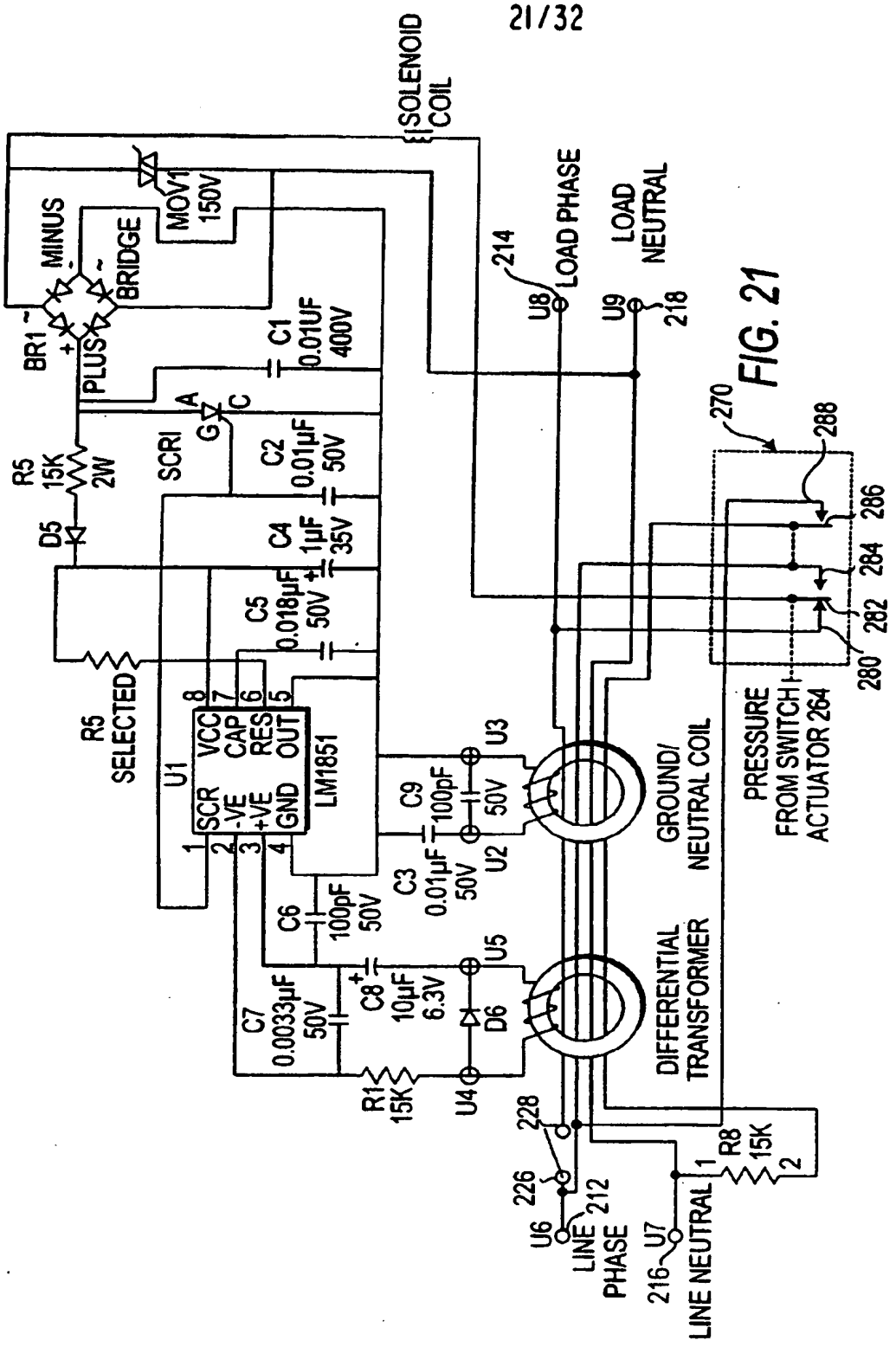

SOLENOID COIL
MOV1 150V
MINUS
BRIDGE
PLUS
BR1
C1 0.01UF 400V
R5 15K 2W
D5
SCR1
C2 0.01µF 50V
C4 1µF 35V
C5 0.018µF 50V
R5 SELECTED
U1
VCC CAP RES OUT
SCR -VE +VE GND
LM1851
C9 100pF 50V
U3
U2
C3 0.01µF 50V
C6 100pF 50V
C7 0.0033µF 50V
C8 10µF 6.3V
D6
U5
U4
R1 15K
U8 LOAD PHASE
U9 LOAD NEUTRAL
214
218
270
288
286
284
282
280
PRESSURE FROM SWITCH ACTUATOR 264
GROUND/ NEUTRAL COIL
DIFFERENTIAL TRANSFORMER
228
226
212
R8 15K
U6 LINE PHASE
U7 LINE NEUTRAL
216

FIG. 21

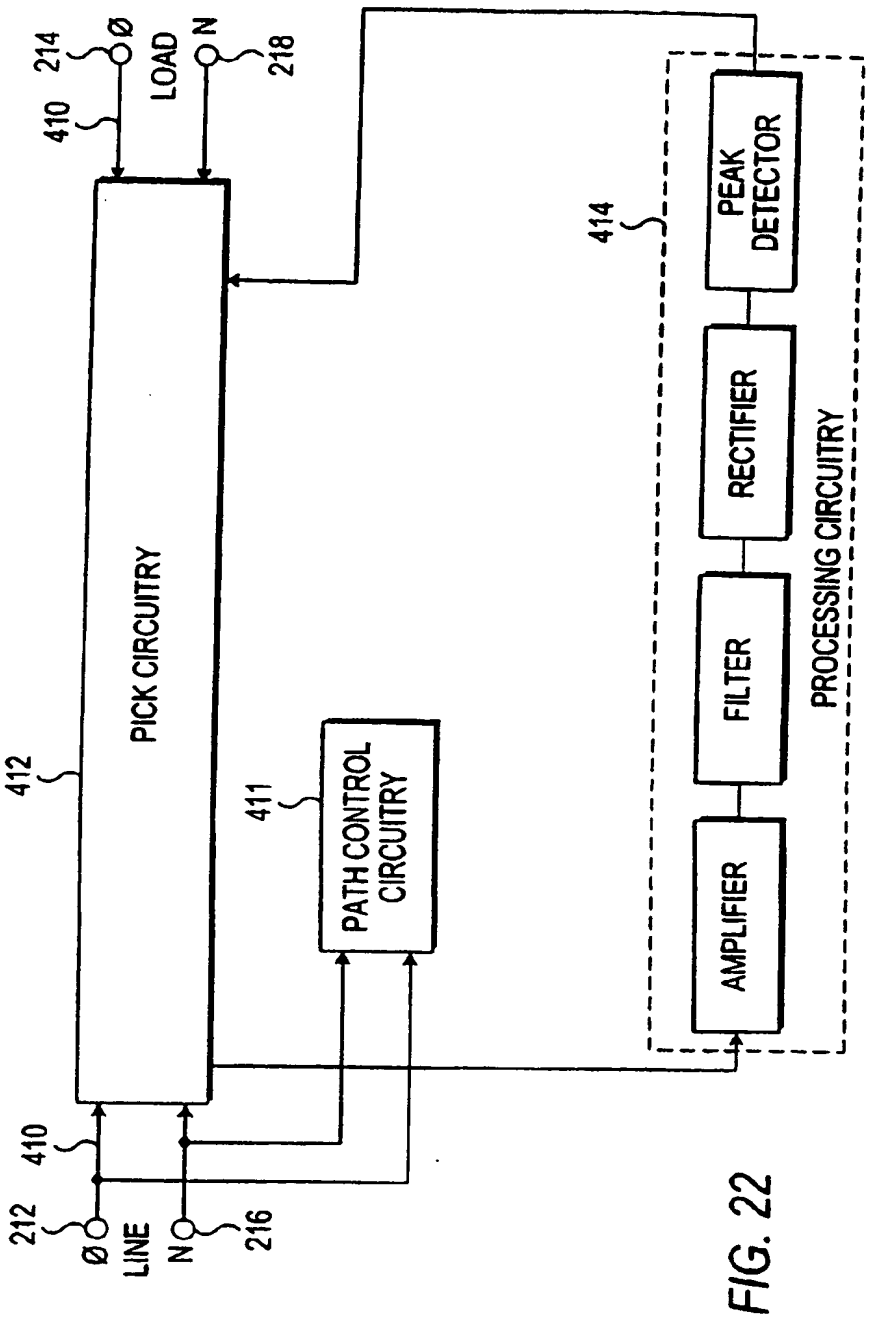

214
Ø
LOAD
N
218
410
PEAK DETECTOR
414
RECTIFIER
FILTER
PROCESSING CIRCUITRY
AMPLIFIER
412
PICK CIRCUITRY
411
PATH CONTROL CIRCUITRY
410
212
Ø
LINE
N
216

FIG. 22

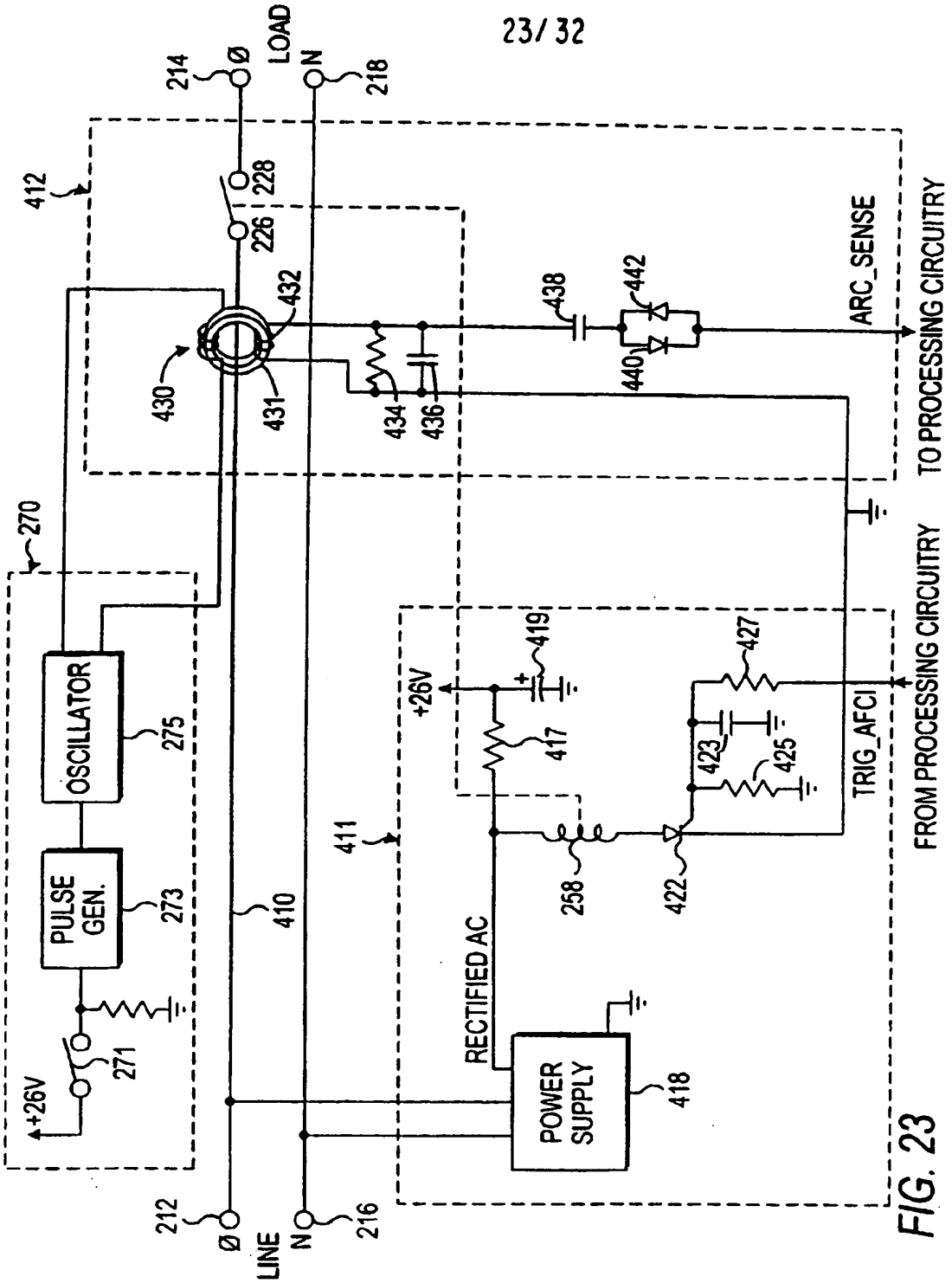

214
Ø
LOAD
N
218
412
228
226
432
438
442
ARC_SENSE
440
430
431
434
436
TO PROCESSING CIRCUITRY
270
OSCILLATOR
275
PULSE GEN.
273
271
+26V
410
411
+26V
419
417
427
423
425
TRIG_AFCI
FROM PROCESSING CIRCUITRY
258
422
RECTIFIED AC
POWER SUPPLY
418
212
Ø
LINE
N
216

FIG. 23

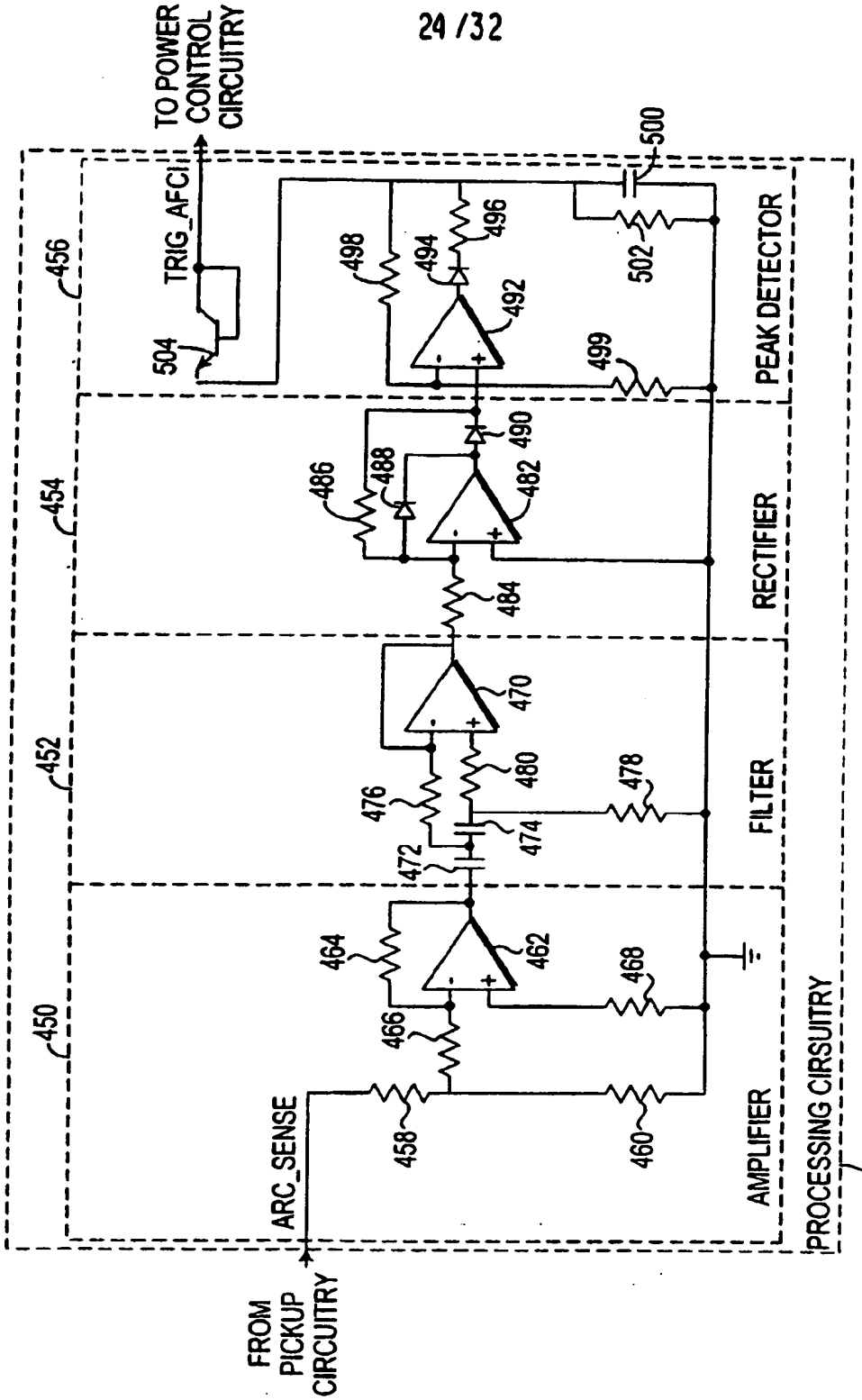

TO POWER CONTROL CIRCUITRY
TRIG_AFCI
504
456
PEAK DETECTOR
500
502
496
498
494
492
499
454
RECTIFIER
490
488
486
482
484
452
FILTER
470
480
478
476
474
472
450
AMPLIFIER
464
462
468
466
458
460
ARC_SENSE
FROM PICKUP CIRCUITRY
PROCESSING CIRSUITRY
414

FIG. 24

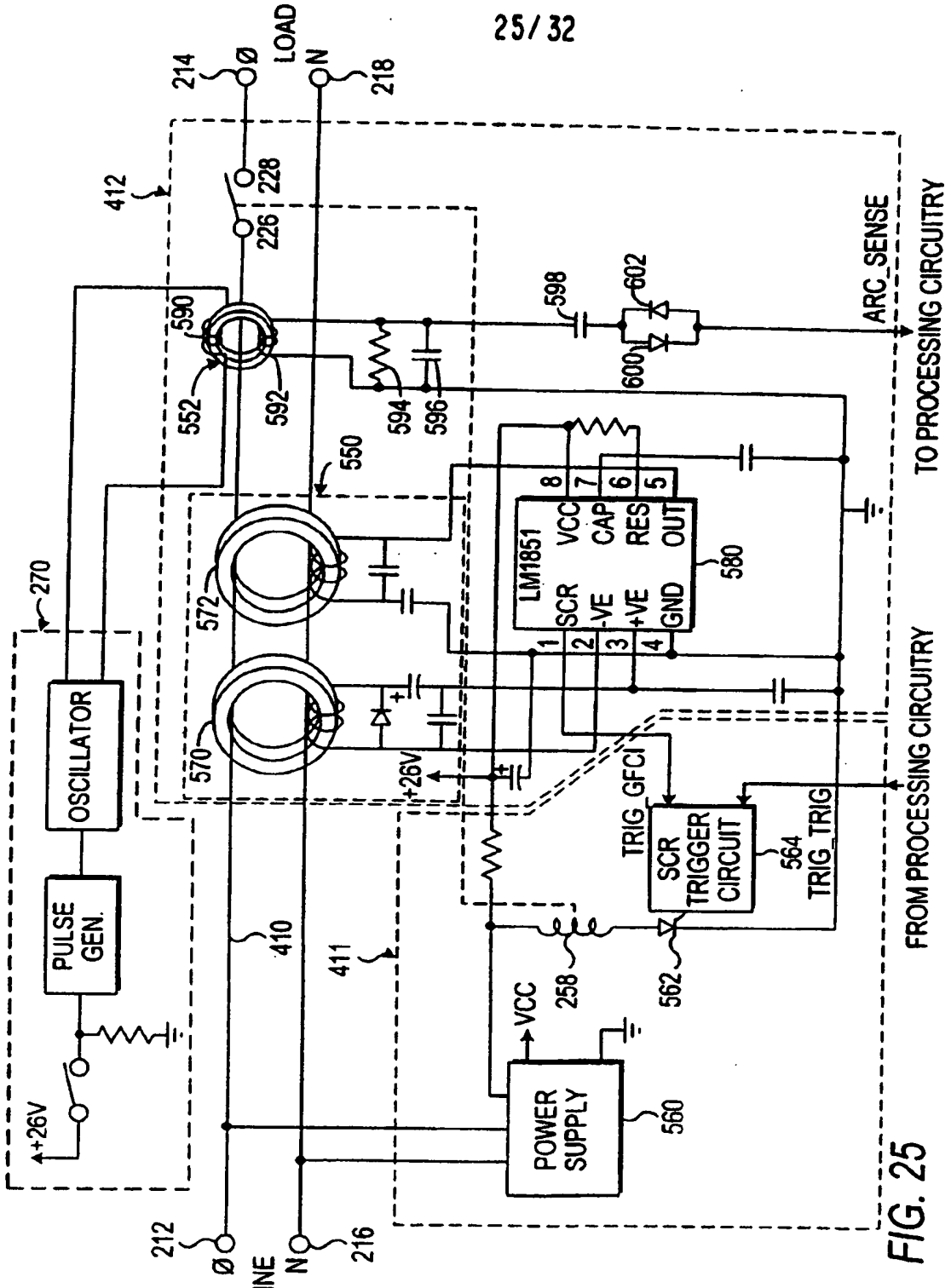

LOAD
214
Ø
N
218
412
228
226
590
552
592
594
596
598
602
600
ARC_SENSE
TO PROCESSING CIRCUITRY
550
LM1851
VCC
CAP
RES
OUT
SCR
-VE
+VE
GND
580
572
570
270
OSCILLATOR
PULSE GEN.
+26V
TRIG_GFCI
SCR TRIGGER CIRCUIT
564
TRIG_TRIG
FROM PROCESSING CIRCUITRY
410
411
258
562
VCC
POWER SUPPLY
560
212
Ø
LINE
N
216

FIG. 25

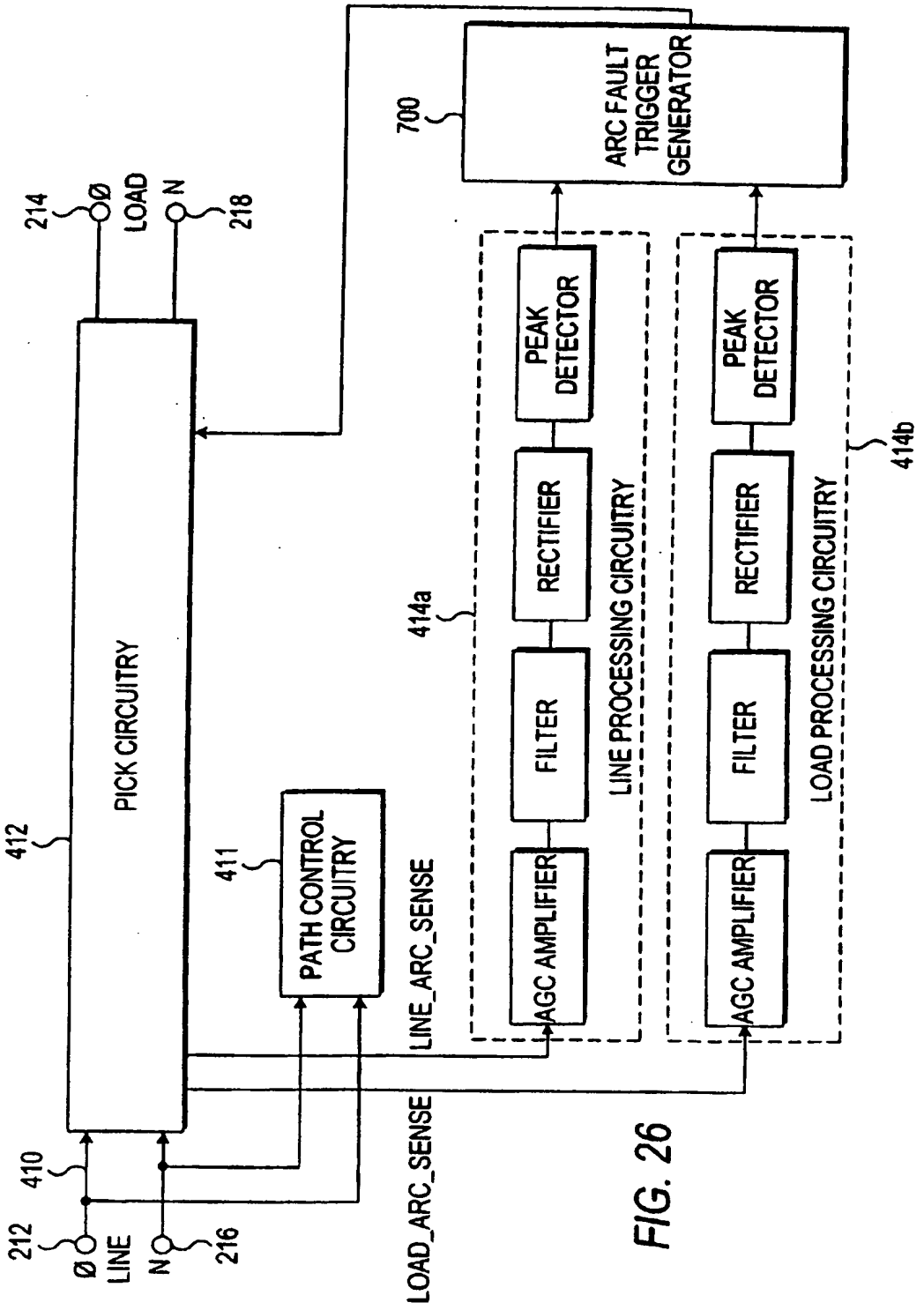

ARC FAULT TRIGGER GENERATOR
700
PEAK DETECTOR
RECTIFIER
FILTER
AGC AMPLIFIER
LINE PROCESSING CIRCUITRY
414a
LOAD PROCESSING CIRCUITRY
414b
PICK CIRCUITRY
412
PATH CONTROL CIRCUITRY
411
LINE_ARC_SENSE
LOAD_ARC_SENSE
214
Ø LOAD
N
218
212
Ø LINE
N
216
410

FIG. 26

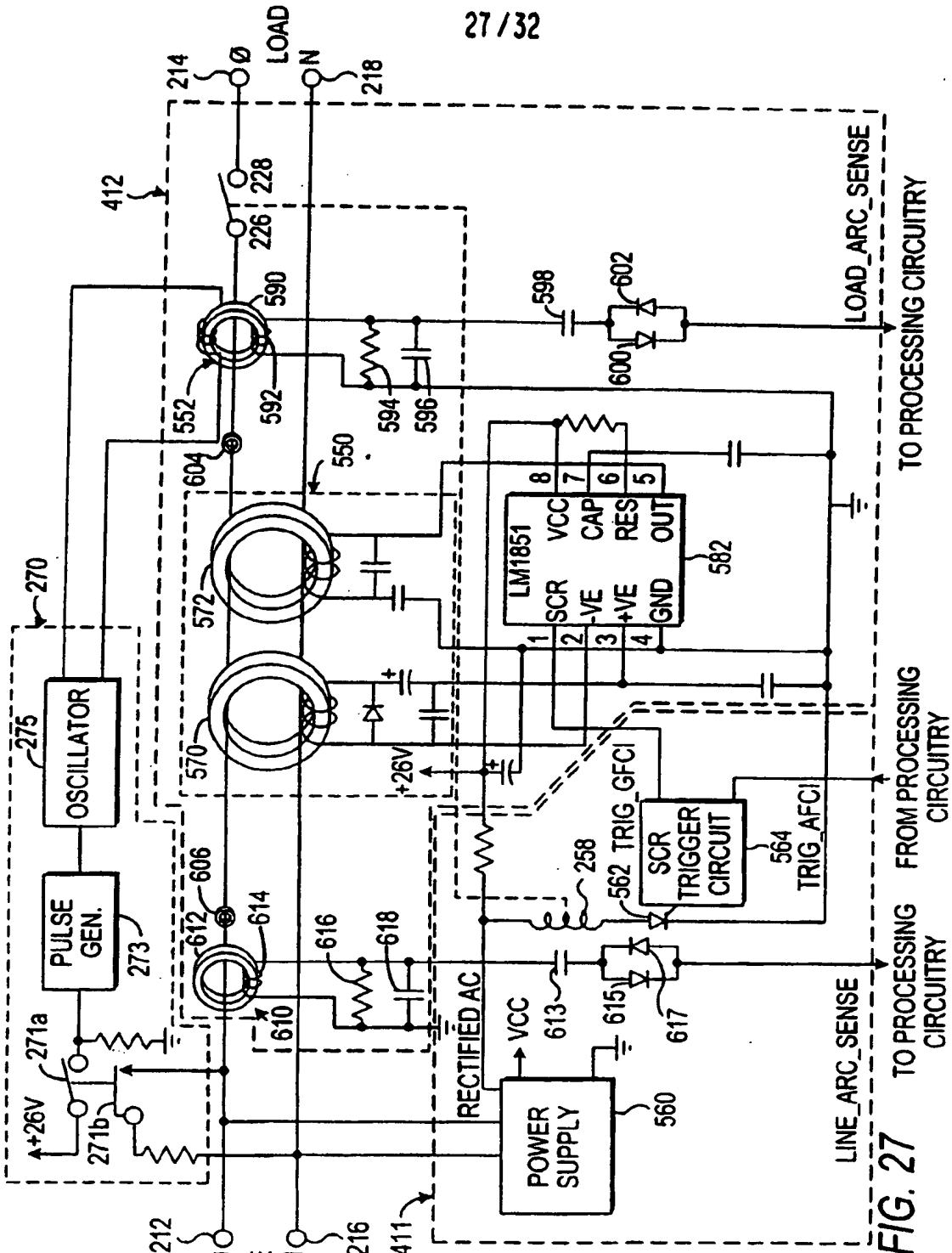

LOAD
Ø
N
214
218
228
226
412
590
552
592
594
596
598
602
600
604
550
572
570
LM1851
VCC
CAP
RES
OUT
SCR
-VE
+VE
GND
582
LOAD_ARC_SENSE
TO PROCESSING CIRCUITRY
270
275
OSCILLATOR
PULSE GEN.
273
271a
271b
+26V
606
612
614
610
616
618
258
562
TRIG_GFCI
SCR TRIGGER CIRCUIT
564
TRIG_AFCI
FROM PROCESSING CIRCUITRY
RECTIFIED AC
VCC
613
615
617
POWER SUPPLY
560
LINE_ARC_SENSE
TO PROCESSING CIRCUITRY
212
Ø
LINE
N
216
411

FIG. 27

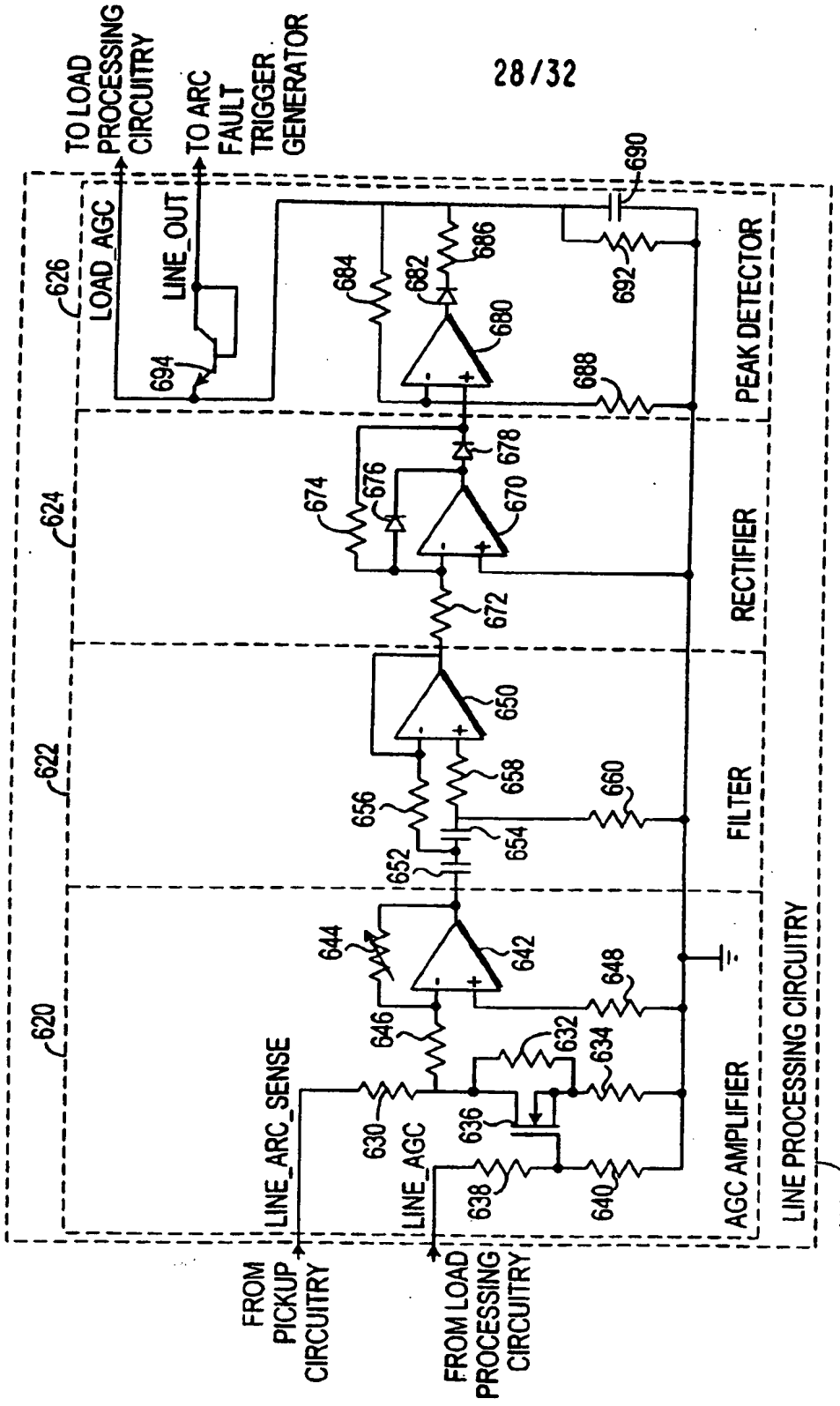

TO LOAD PROCESSING CIRCUITRY
TO ARC FAULT TRIGGER GENERATOR
LOAD_AGC
LINE_OUT
626
624
622
620
694
684
682
686
680
690
692
688
678
676
674
670
672
650
658
656
660
654
652
644
642
648
646
632
634
630
636
638
640
LINE_ARC_SENSE
LINE_AGC
FROM PICKUP CIRCUITRY
FROM LOAD PROCESSING CIRCUITRY
PEAK DETECTOR
RECTIFIER
FILTER
AGC AMPLIFIER
LINE PROCESSING CIRCUITRY
414a

FIG. 28

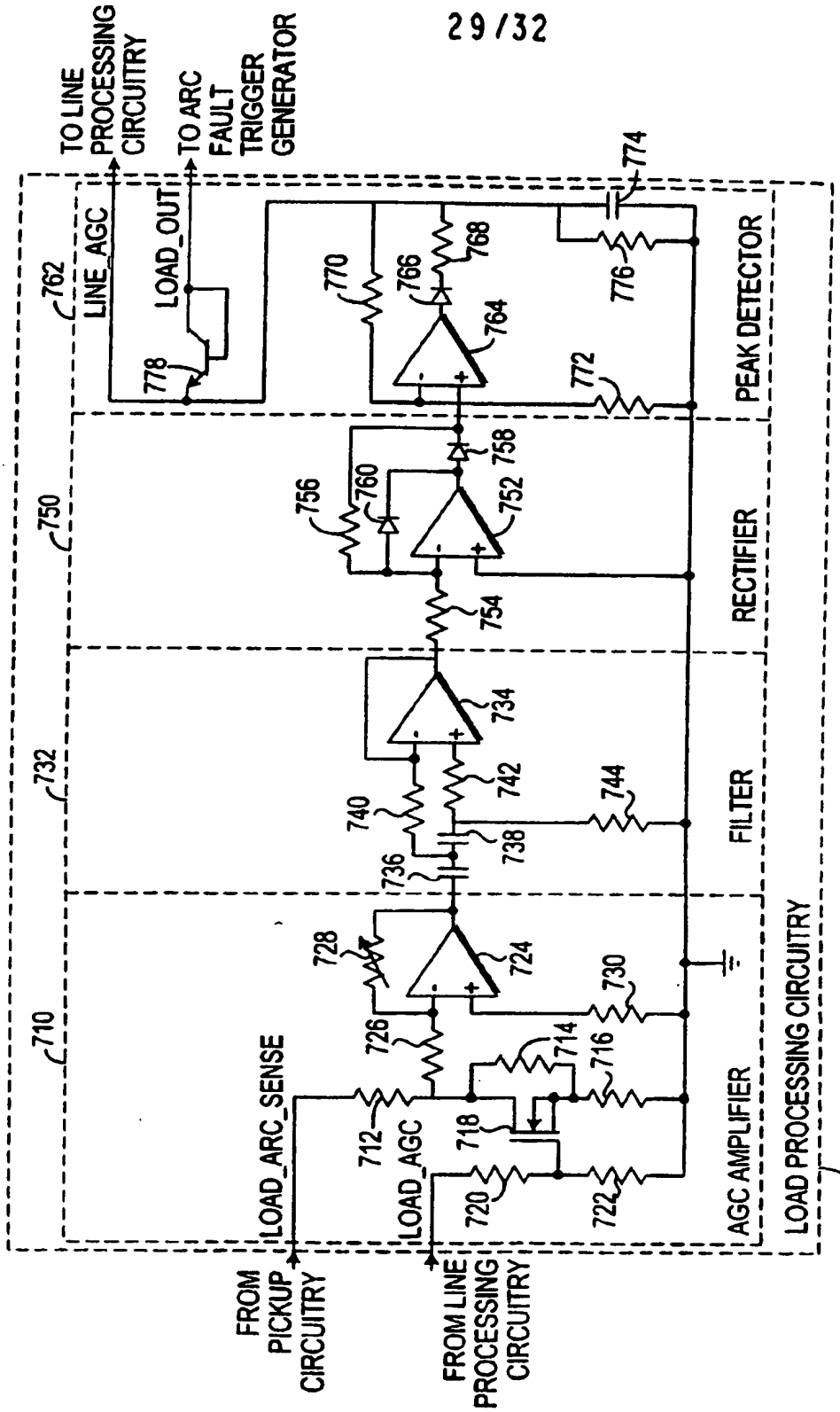

TO LINE PROCESSING CIRCUITRY
TO ARC FAULT TRIGGER GENERATOR
LINE_AGC
LOAD_OUT
762
778
770
766
768
764
772
774
776
PEAK DETECTOR
750
756
760
758
752
754
RECTIFIER
732
734
740
742
744
738
736
FILTER
710
728
724
730
726
714
716
712
718
720
722
LOAD_ARC_SENSE
LOAD_AGC
AGC AMPLIFIER
LOAD PROCESSING CIRCUITRY
414b
FROM PICKUP CIRCUITRY
FROM LINE PROCESSING CIRCUITRY

FIG. 29

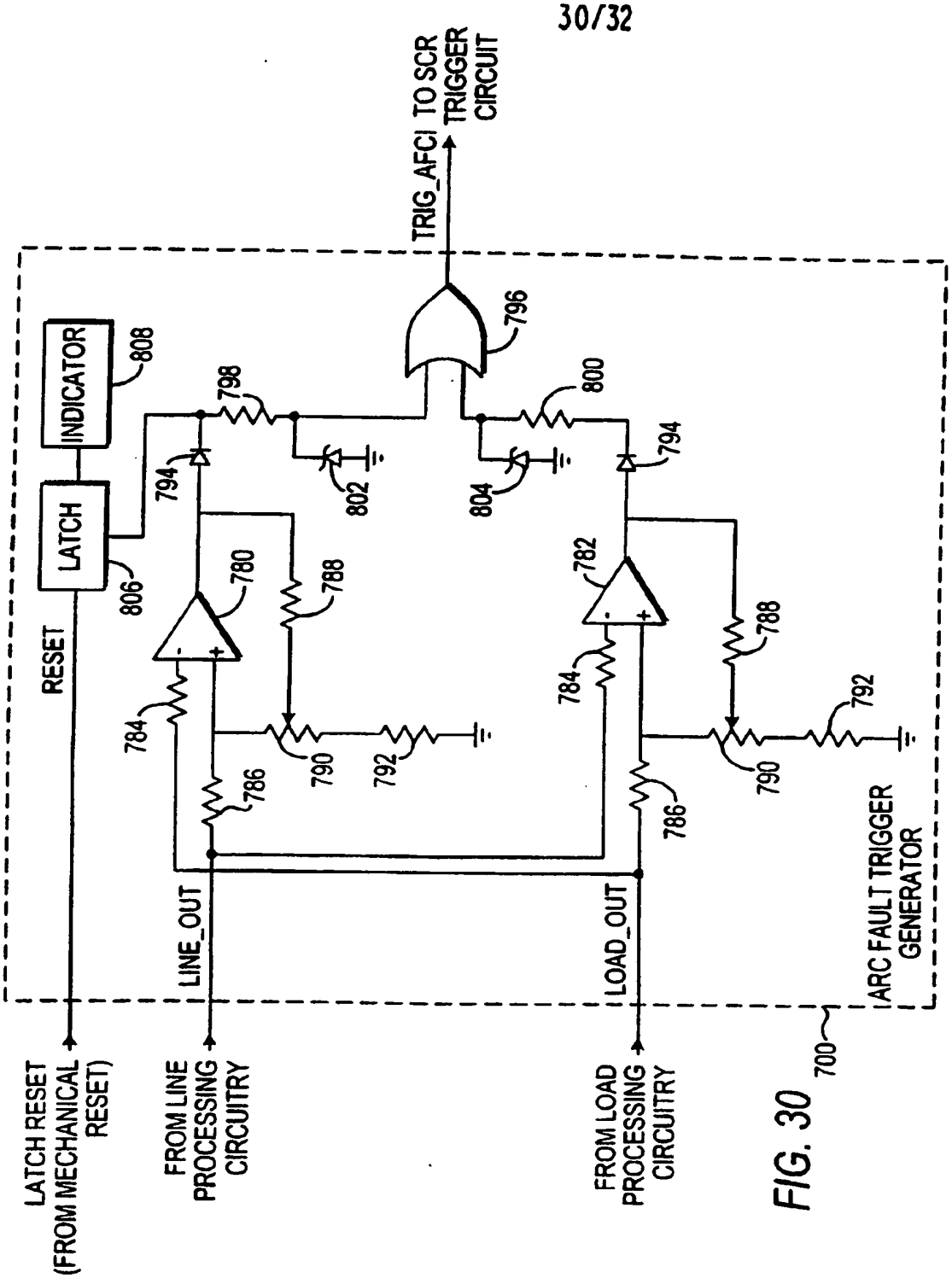

TRIG_AFCI
TO SCR TRIGGER CIRCUIT
796
INDICATOR
808
LATCH
806
RESET
798
800
794
802
804
780
782
788
784
786
790
792
LINE_OUT
LOAD_OUT
ARC FAULT TRIGGER GENERATOR
700
LATCH RESET (FROM MECHANICAL RESET)
FROM LINE PROCESSING CIRCUITRY
FROM LOAD PROCESSING CIRCUITRY

FIG. 30

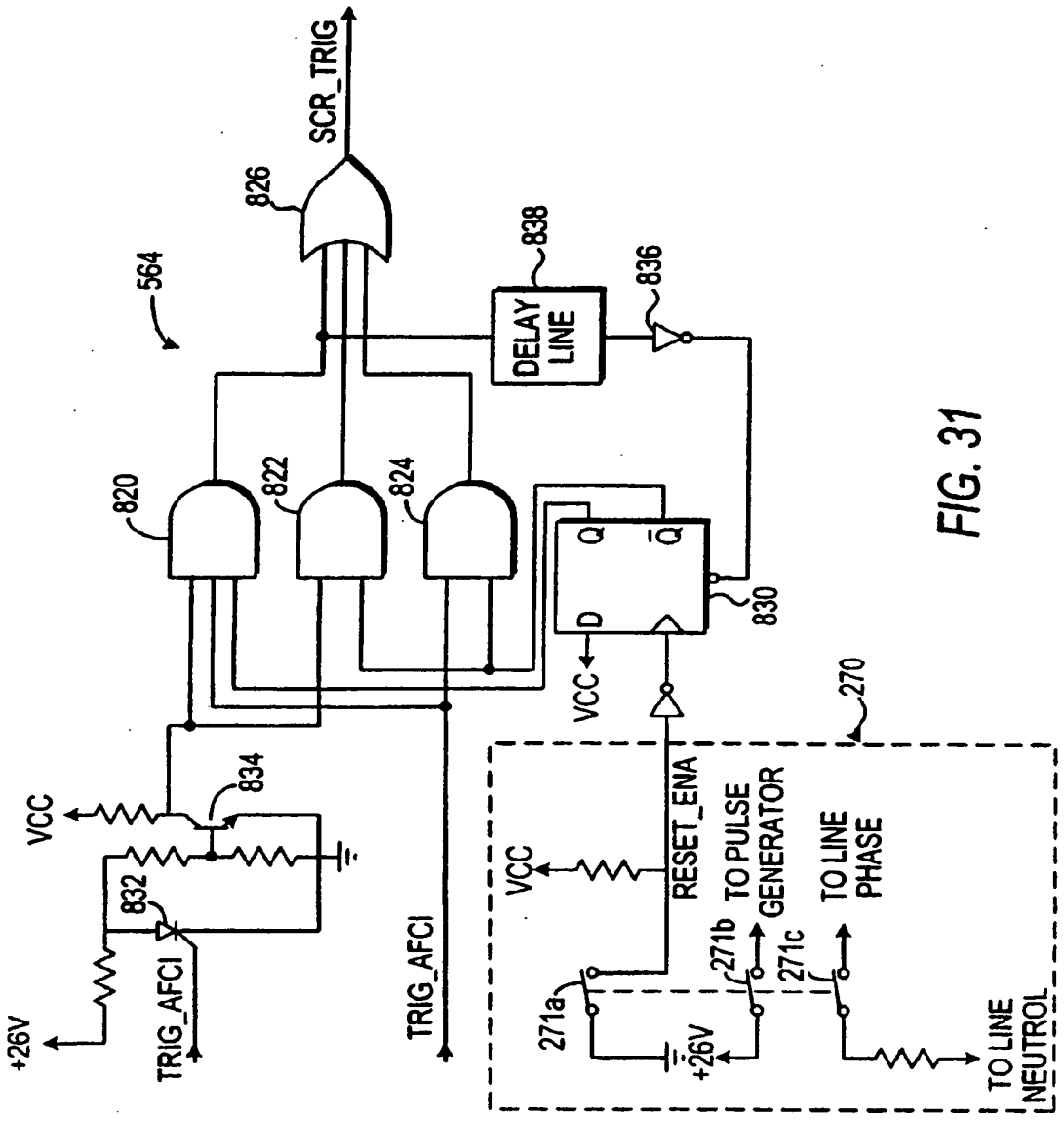
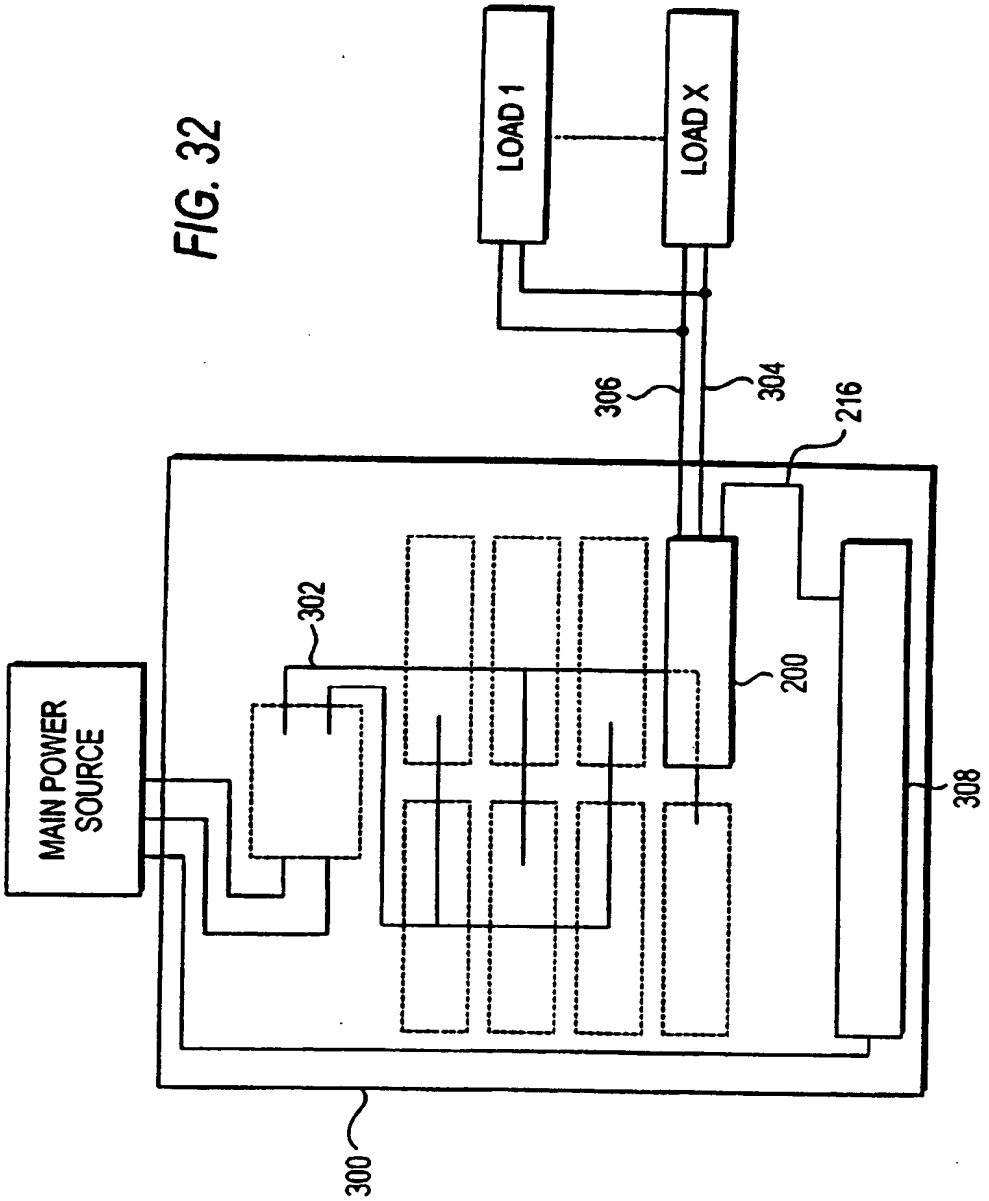

SCR_TRIG
826
564
838
DELAY LINE
836
820
822
824
Q
Q
D
830
VCC
270
834
VCC
832
RESET_ENA
TO PULSE GENERATOR
TO LINE PHASE
VCC
271b
271c
271a
+26V
TRIG_AFCI
TRIG_AFCI
+26V
TO LINE NEUTROL

FIG. 31

FIG. 32



This Page is Inserted by IFW Indexing and Scanning Operations and is not part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- ☑ BLACK BORDERS
- ☐ IMAGE CUT OFF AT TOP, BOTTOM OR SIDES
- ☐ FADED TEXT OR DRAWING
- ☐ BLURRED OR ILLEGIBLE TEXT OR DRAWING
- ☐ SKEWED/SLANTED IMAGES
- ☐ COLOR OR BLACK AND WHITE PHOTOGRAPHS
- ☐ GRAY SCALE DOCUMENTS
- ☑ LINES OR MARKS ON ORIGINAL DOCUMENT
- ☐ REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY
- ☐ OTHER: _____

IMAGES ARE BEST AVAILABLE COPY.
As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.